IPC-7251
Generic Requirements for Through-Hole Design and Land Pattern Standard

1st Working Draft – June 2008

1 SCOPE

This document provides information on land pattern geometries used for the through-hole attachment of electronic components. The intent of the information presented herein is to provide the appropriate size, shape and tolerance of through land patterns to insure sufficient area for the appropriate solder fillet around the lead to meet the requirements of IPC/EIA J-STD-001 and the workmanship standard IPC-A-610, and also to allow for inspection, testing, and rework of those solder joints.

1.1 Purpose Although, in many instances, the land pattern geometries can be different based on the type of soldering used to attach the electronic part, wherever possible, land patterns are defined with consideration to the attachment process being used. Designers can use the information contained herein to establish standard configurations not only for manual designs but also for computer-aided design systems. Whether parts are subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

Land patterns are dimensionally defined and are a part of the printed board (PB) circuitry geometry, as they are subject to the producibility levels and tolerances associated with plating, etching, assembly or other conditions. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns.

Note 1: The dimensions used for component descriptions have been extracted from standards developed by industrial and/or standards bodies. Designers should refer to these standards for additional or specific component package dimensions.

Note 2: For a comprehensive description of the given PB and for achieving the best possible solder connections to the devices assembled, the whole set of design elements includes, beside the land pattern definition:

- Solder mask
- Solder paste stencil
- Clearance between adjacent components
- Clearance between bottom of component and PB surface, if relevant
- Keepout areas, if relevant
- Suitable rules for adhesive applications

The whole of design elements is commonly defined as ‘‘mounting conditions.’’ This standard defines land patterns and includes recommendations for clearances between adjacent components and for other design elements.

Note 3: Elements of the mounting conditions, particularly the courtyard, given in this standard are related to the reflow soldering process. Adjustments for wave or other soldering processes, if applicable, have to be carried out by the user. This may also be relevant when solder alloys other than eutectic tin lead solders are used.

Note 4: Heat dissipation aspects have not been taken into account in this standard. Greater mass may require slower process speed to allow heat transfer.

Note 5: Heavier components (greater weight per land) require larger lands; thus, adding additional land pattern surface will increase surface area of molten solder to enhance capabilities of extra weight. In some cases the lands shown in the standard may not be large enough; in these cases, considering additional measures may be necessary.

1.2 Documentation Hierarchy This standard identifies the generic physical design principles involved in the creation of land patterns for through-hole components, and is supplemented by a shareware IPC Land Pattern Viewer that provides, through the use of a graphical user interface, the individual component dimensions and corresponding land pattern recommendations based upon families of components. The IPC Land Pattern Viewer is provided on CD-ROM as part of this standard. Updates to land pattern dimensions, including patterns for new component families, can be found on the IPC website (www.ipc.org) under ‘‘PCB Tools and Calculators.’’ See Appendix A for more information on the IPC Land Pattern Viewer.

1.2.1 Component and Land Pattern Family Structure The IPC-7251 provides the following number designation within this standard for each major family of through-hole components to indicate similarities in solder joint engineering goals:

IPC-7252 – Discrete Components (Axial and Radial Leaded Components)
IPC-7253 – Dual-in-Line Package (DIP)

IPC-7254 – Three Leaded Semiconductor
IPC-7255 – Pin Grid Array
IPC-7256 – Unique Multiple Function Parts
IPC-7257 – Connectors and Headers
IPC-7258 – Single Inline Package (SIP) Resistor Networks
IPC-7259 – Mounting Hardware

Note: None of the families provided above are intended for release as separate publications from this standard. They are intended for classification purposes only within this standard.

1.3 Performance Classification Three general end-product classes have been established to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there may be an overlap of equipment between classes.

The end product user has the responsibility for determining the ''Use Category'' or ''Class'' to which the product belongs. The contract between user and supplier shall specify the ''Class'' required and indicate any exceptions or additional requirements to the parameters, where appropriate.

Class 1 General Electronic Products – Includes consumer products, some computer and computer peripherals, and hardware suitable for applications where the major requirement is function of the completed assembly.

Class 2 Dedicated Service Electronic Products Includes communications equipment, sophisticated business machines, and instruments where high performance and extended life is required, and for which uninterrupted service is desired but not mandatory. Typically the end-use environment would not cause failures.

Class 3 High Reliability Electronic Products – Includes all equipment where continued performance or performance-on-demand is mandatory. Equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support systems and other critical systems.

The IPC-7251 land patterns have the capability of accommodating all three performance classifications.

1.3.1 Producibility Levels When appropriate this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

Level A General Design Producibility – Preferred [Maximum land/lead to hole relationship]
Level B Moderate Design Producibility – Standard [Nominal land/lead to hole relationship]
Level C High Design Producibility – Reduced [Least land/lead to hole relationship]

The producibility levels are not to be interpreted as a design requirement, but a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the tables of IPC-7251 are used in the IPC Land Pattern Viewer and are a guide in determining what the level of producibility will be for any feature. The specific requirement for any feature that must be controlled on the end item shall be specified on the master drawing of the PB or the PB assembly drawing.

1.4 Land Pattern Determination This standard discusses two methods of providing information on land patterns and hole configurations:

1. Exact details based on industry component specifications, PB manufacturing and component placement accuracy capabilities. These land patterns are restricted to a specific component, and have an identifying IPC-7251 land pattern name.
2. Equations can be used to alter the given information to achieve a more robust solder connection, when used in particular situations where the equipment for placement or attachment are more or less precise than the assumptions made when determining the land pattern details (see 3.1.2).

Three land pattern, hole size, and lead extension geometry variations are supplied for each of the device families:

Level A: Maximum Land/Lead to Hole Relationship – The 'maximum' land pattern conditions have been developed to accommodate the most robust producibility of the solder application method. The geometry furnished may provide a wider process window for solder processes as well. The Level A land patterns are normally considered for low component density product applications.

Level B: Nominal Land/Lead to Hole Relationship –The nominal land patterns furnished for all device families will provide a robust solder attachment condition for most soldering processes and should provide a condition suitable for wave, dip, drag or reflow soldering. Products with a moderate level of component density may consider adapting the 'nominal' land pattern geometry.

Level C: Least Land/Lead to Hole Relationship –Selection of the minimum land pattern geometry may not be suitable for all product use categories. High component density typical of portable and hand-held product applications may consider the 'minimum' land pattern geometry variation.

The use of classes of performance (1, 2, and 3) is combined with that of levels (A, B, and C) in explaining the condition of an electronic assembly. As an example, combining the description as Levels 1A or 3B or 2C, would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular assembly.

Although all three land pattern geometry variations are considered compliant for lead free soldering processes, the Level C variant will require more process control to ensure a proper wetting of the lead free alloy. It is important to note, however, that the primary issue of lead free relates to the surface finish on the PB and the component termination. See 3.2.3 for further information on land pattern design in lead free soldering environments.

1.5 Terms and Definitions

Terms and definitions used herein are in accordance with IPC-T-50 except as otherwise specified.

Note: Any definition denoted with an asterisk (*) is a reprint of the term defined in IPC-T-50.

***Assembly** – A number of parts, subassemblies or combinations thereof joined together. (Note: This term can be used in conjunction with other terms listed herein, e.g., ''Printed Board Assembly.'')

Assembly, Double-Sided – Packaging and interconnecting structure with components mounted on both the primary and secondary sides.

Assembly, Multilayer Printed Circuit (Wiring) – Multilayer printed circuit or printed wiring board on which separately manufactured components and parts have been added.

Assembly, Packaging and Interconnecting (P&IA) – Generic term for an assembly that has electronic components mounted on either one or both sides of a packaging and interconnecting structure.

Assembly, Printed Board – An assembly of several printed circuit assemblies or printed wiring assemblies, or both.

Assembly, Printed Circuit (Wiring) – A printed circuit or printed wiring board on which separately manufactured components and parts have been added.

Assembly, Single-Sided – Packaging and interconnecting structure with components mounted only on the primary side.

***Base Material** – The insulating material upon which a conductive pattern may be formed. (The base material may be rigid or flexible, or both. It may be a dielectric or insulated metal sheet.)

***Basic Dimension** – A numerical value used to describe the theoretical exact location of a feature or hole. (It is the basis from which permissible variations are established by tolerance on other dimensions in notes or by feature control symbols.)

***Blind Via** – A via extending only to one surface of a PB.

***Buried Via** – A via that does not extend to the surface of a PB.

Coefficient of Thermal Expansion (CTE) – The linear dimensional change of a material per unit change in temperature. (See also ''Thermal Expansion Mismatch.'')

***Component** – An individual part or combination of parts that, when together, perform a design function(s). (See also ''Discrete Component.'')

Component Mounting Site – The location on a Package Interconnect (P&I) structure that consists of a land pattern and conductor fan-out to additional lands for testing or vias that are associated with the mounting of a single component.

Conductive Pattern – The configuration or design of the conductive material on a base material. (This includes conductors, lands, vias, heatsinks and passive components when these are an integral part of the PB manufacturing process.)

Conductor – A single conductive path in a conductive pattern.

Constraining Core – A supporting plane that is internal to a packaging and interconnecting structure.

Courtyard – The smallest polygon area that provides a minimum electrical and mechanical clearance (courtyard excess) around the combined component body and land pattern boundaries.

Courtyard Excess – The area between the polygon circumscribing the land pattern and the component, and the outer boundary of the courtyard. The courtyard excess may be different in the x-and y-direction.

Courtyard Manufacturing Zone – The area that provides a minimum electrical and mechanical clearance (courtyard excess) around the combined component body and land pattern boundaries.

Dual-Inline Package (DIP) – A basically-rectangular component package that has a row of leads extending from each of the longer sides of its body that are formed at right angles to a plane that is parallel to the base of its body.

Fiducial (Mark) – A PB artwork feature(s) that is created in the same process as the conductive pattern and that provides a common measurable point for component mounting with respect to a land pattern or land patterns.

Footprint – See ‘‘Land Pattern.’’

Grid – An orthogonal network of two sets of parallel equidistant lines that is used for locating points on a PB.

Integrated Circuit (IC) – A combination of inseparable associated circuit elements that are formed in place and interconnected on or within a single base material to perform a particular electrical function.

Intrusive Soldering – A process in which the solder paste for the through-hole components is applied using a stencil or syringe to accommodate through-hole components that are inserted and reflow-soldered together with the surface-mount components.

Jumper wire – A discrete electrical connection that is part of the original design and is used to bridge portions of the basic conductive pattern formed on a PB.

Land – A portion of a conductive pattern usually used for the connection and/or attachment of components.

Land Pattern – A combination of lands that is used for the mounting, interconnection and testing of a particular component.

Master Drawing – A control document that shows the dimensional limits or grid locations that are applicable to any and all parts of a product to be fabricated, including the arrangement of conductors and nonconductive patterns or elements; the size, type, and location of holes; and all other necessary information.

Mixed Component-Mounting Technology – A component mounting technology that uses both through-hole and surface-mounting technologies on the same packaging and interconnecting structure.

Module – A separable unit in a packaging scheme.

Nominal Dimension – A dimension that is between the maximum and minimum size of a feature. (The tolerance on a nominal dimension gives the limits of variation of a feature size.)

Packaging and Interconnecting Structure (P&IS) – The general term for a completely processed combination of base materials, supporting planes or constraining cores, and interconnection wiring that are used for the purpose of mounting and interconnecting components.

Plated-Through Hole (PTH) – A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layer, or both, of a PB.

Primary Side – The side of a packaging and interconnecting structure that is so defined on the master drawing. (It is usually the side that contains the most complex or the most number of components.)

Printed Board (PB) – The general term for completely processed printed circuit and printed wiring configurations. (This includes single-sided, double-sided and multilayer boards with rigid, flexible, and rigid-flex base materials.)

Printed Wiring – A conductive pattern that provides point-to-point connections but not printed components in a predetermined arrangement on a common base. (See also ‘‘Printed Circuit.’’)

Registration – The degree of conformity of the position of a pattern (or portion thereof), a hole, or other feature to its intended position on a product.

Secondary Side – That side of a packaging and interconnecting structure that is opposite the primary side. (It is the same as the ‘‘solder side’’ on through-hole mounting technology.)

Single-Inline Package (SIP) – A component package with one straight row of pins or wire leads.

Static Charge – An electrical charge that has accumulated or built up on the surface of a material

Static Electricity Control – A technique where materials and systems are employed to eliminate/discharge static electricity build-up by providing continuous discharge paths

Supported Hole – A hole in a PB that has its inside surfaces plated or otherwise reinforced.

Supporting Plane – A planar structure that is a part of a packaging and interconnecting structure in order to provide mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical characteristics. (It may be either internal or external to the packaging and interconnecting structure.) (See also ‘‘Constraining Core.’’)

Surface Mount Technology (SMT) – The electrical connection of components to the surface of a conductive pattern that does not utilize component holes.

Tented Via (Type I Via) – A via with a mask material (typically dry film) applied bridging over the via wherein no additional materials are in the hole. It may be applied to one side or both.

Thermal Mismatch – The absolute difference between the thermal expansion of two components or materials. (See also ‘‘Coefficient of Thermal Expansion (CTE).’’)

Through Connection – The electrical connection to connect conductor patterns on the front side through to the back side of a PB. (See also ‘‘Interfacial Connection.’’)

Through-Hole Technology (THT) – The electrical connection of components to a conductive pattern by the use of component holes.

Tooling Feature – A physical feature that is used exclusively to position a PB or panel during a fabrication, assembly or testing process. (See also ‘‘Locating Edge,’’ ‘‘Locating Edge Marker,’’ ‘‘Locating Notch,’’ ‘‘Locating Slot,’’ and ‘‘Tooling Hole.’’)

Unsupported Hole – A hole in a PB that does not contain plating or other type of conductive reinforcement.

Via – A plated-through hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material. (See also ‘‘Blind Via’’ and ‘‘Buried Via.’’)

2 APPLICABLE DOCUMENTS

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-A-610 Acceptability of Printed Board Assemblies

IPC-1902 Grid System for Printed Circuits

IPC-2221 Generic Standard on Printed Board Design

IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards

IPC-2226 Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

IPC-2511 Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer Methodology

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

IPC-4761 Design Guide for Protection of Printed Board Via Structures

IPC-6012 Qualification and Performance Standard for Rigid Printed Boards

IPC-7525 Stencil Design Guidelines

IPC-7530 Guidelines for Temperature Profiling for Mass Soldering Processes

IPC-7711/21 Rework and Repair Guide

2.2 Electronic Industries Association[2]

EIA-481 Tape and Reel Specification

2.3 Joint Industry Standards (IPC)[1]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Tests for Printed Boards

J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

J-STD-033 Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

2.4 International Electrotechnical Commission[3]

IEC-61188 Printed Boards and Printed Board Assemblies Design and Use

2.5 Joint Electron Device Engineering Council (JEDEC)[4]

Publication 95 JEDEC Registered and Standard Outlines for Solid State Products

1. www.ipc.org
2. www.eia.org
3. www.iec.ch
4. www.jedec.org

3 DESIGN REQUIREMENTS

3.1 Dimensioning Systems This section describes a set of dimensional criteria for components, land patterns, positional accuracy of the component placement capability and the opportunity to create a certain size solder joint commensurate with reliability or product performance analysis.

Maximum boundary tolerances for through-hole components consider the maximum land sizes and maximum component outlines. These dimensions are sufficient in order to control the amount of space needed to accommodate component placement without interference, provided that the recommended courtyard excess around the boundary is maintained. It is also recommended that an additional manufacturing excess is added to the courtyard, however those characteristics are not included in this standard, and each design needs to consider the amount of excess room needed for component replacement or testing. Each component family shows the unique characteristics used in determining the component and land pattern image.

Land pattern etch factors, location of features, and positional accuracy are assumed as the nominal dimensions provided in the IPC-2220 design standards, with no additional allowances incorporated since sufficient variations have been built into the calculation methods based on the maximum boundary determinations.

Tolerances used in the dimensioning system to define the maximum size range of the component, land, lead diameter and lead extensions dimensions are used without ambiguity. The intent of using these boundaries is to accommodate the

placement equipment heads as shown in Figure 3-1. Thus the maximum boundary descriptions provide for the equipment tooling clearance needed in automated assembly.

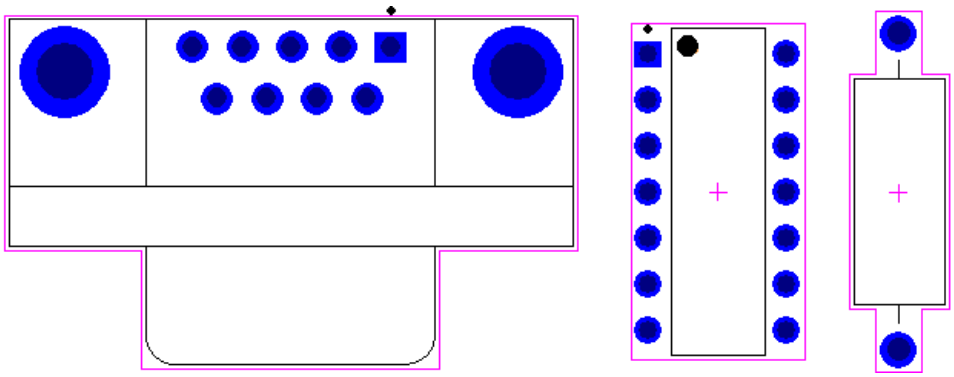


Figure 3-1 Tolerancing Method

The use of a set of requirements are adopted and invoke the following rules, as defined in IPC-2615 unless otherwise modified:

a. All location dimensions are basic (nominal)
b. All feature dimensions are at Maximum Material Condition (MMC)
c. Limits of size control form as well as size
d. Perfect form is required at maximum dimensions
e. Datum references and position tolerances apply at maximum dimensions, and are dependent on feature size
f. Position dimensions originate from maximum dimensions
g. Tolerances and their datum references other than size and position apply regardless of feature size (RFS)

The dimensioning concepts used for this system of analysis consider the assembly/attachment requirements as their major goal. Specification (data) sheets for components or dimensions for land patterns on PBs may use different dimensioning concepts, however, the goal is to combine all concepts into a single system. Users are encouraged to establish the appropriate relationship between their dimensioning system(s) and the dimensioning system and analysis concepts described herein to allow for ease of tailoring these concepts for robust process performance. As an example, if the tolerance used for positioning is larger than the machine tolerance used in production, a single dimensional change could modify the land pattern.

3.1.1 Component Tolerancing The component manufacturers and industry standards organizations are responsible for the dimensioning and tolerancing of electronic components (see 3.1.5.2). The basic dimensions and tolerance limits published in the specifications have been converted to a functional equivalent using the MMC tolerancing method with all components shown with their MMC dimensional limit (maximum size). Tolerances are bilateral, and are described to reflect the best condition for solder joint formation and physical clearance.

The concept for component dimension evaluations is based on the type of component style, the maximum body dimensions, and the lead terminal extension conditions as shown in Figure 3-2, and considered at the maximum characteristics involved in the formation of the acceptable solder joint.

Component manufacturers provide dimensions for their parts showing either the limits of size (max/min) or they provide a nominal size and then put a tolerance on that nominal dimension. In order to facilitate the dimensioning system, these dimensions and their associated tolerances are converted to minimum and maximum size. If only a nominal dimension is provided the variation on the dimension must be determined empirically in order to establish the appropriate land pattern.

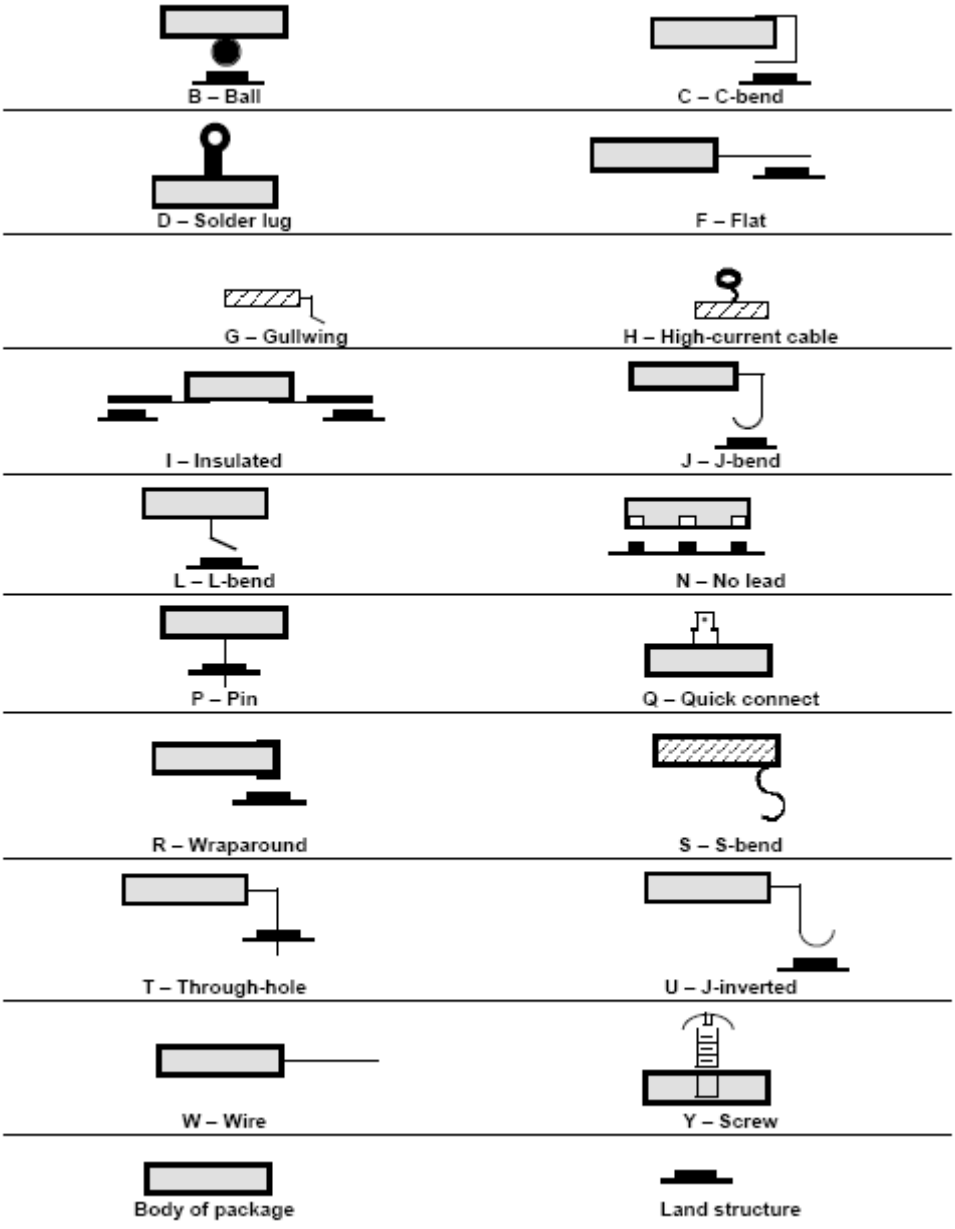
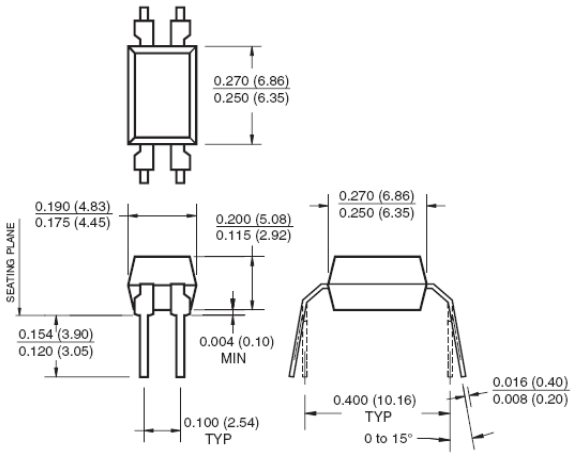


Figure A.1 — Illustrations of lead form (or terminal shape)

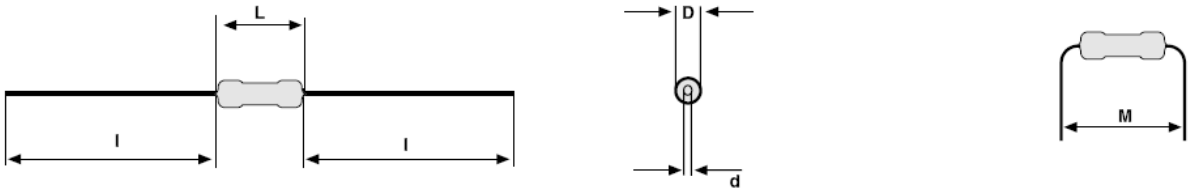
Figure 3-2 Lead Body Exit Position

Figure 3-3 and Figure 3-4 show an example of what might be contained in a component data sheet and how the land pattern and maximum boundaries are determined. It should be noted that in many instances the level of complexity changes for each component description based on the analysis factors that influence the amount of room required for each component style. At times this influence is based on a variation of the land to hole relationship; at other times it may be based on lead bending requirements.



Body = 4.83 uses 5.0 mm for component width maximum boundary
Land Area – 10.16 + 1.0 mm maximum land (Nominal Land Pattern) uses 11.20 component length for boundary
Courtyard excess is determined by the appropriate table in 3.1.5.1
Level A = 6.0 x 12.2 Level B = 5.6 x 11.8 Level C = 5.2 x 11.4 [Note Level B has been extended to make the centroid dimension even]

Figure 3-3 DIP Component Dimensioning Example



Body diameter = 1.6 max
Lead diameter = 0.5 nominal
Land/lead to hole relationship = Level A = 1.2 hole/2.8 land; Level B = 1.0 hole/2.4 land; Level C = 0.8 hole/2.0 land
Body Length = 3.6 + minimum lead extension = 2.4 Level A; 2.0 Level B and 1.6 Level C + land
Maximum length boundary dimension = Level A 8.8; Level B 8.0; Level C 7.2

Figure 3-4 Axial Leaded Component Dimensioning Example

3.1.2 Land Tolerancing All tolerances for lands are intended to provide a projected land pattern with individual lands at maximum size. Etching tolerances are intended to reduce the land size and thus result in a lesser area for solder joint formation. In order to facilitate component hole location and tolerancing, the land pattern dimensioning system considers the annular ring hole size and a manufacturing allowance that prevents hole breakout of the land pattern as required by IPC-2221.

The dimensioning concept in this standard uses geometric tolerancing to describe the allowable dimensions of the land pattern and encompasses the maximum characteristics in order to accommodate the manufacturing variations. When lands are at their maximum size, the result may be a minimum acceptable space between lands; conversely when lands are at their minimum size, the result may be a minimum acceptable land pattern necessary to achieve the minimum required hole to land relationship. These thresholds allow for gauging of the land pattern for go/no-go conditions. The whole concept of the dimensioning system described in this document is based on these principles and extends to component mounting dimensions, land pattern dimensions, positioning dimensions, etc., so that the requirements may be examined using optical gauges at any time in the process in order to insure compliance with the tolerance analysis (see Table 3-1).

3.1.3 Fabrication Allowances IPC-2221provides the minimum fabrication allowance associated with the hole/land relationship. This allowance considers production master tooling and process variations required to fabricate PBs. Each dimension given is considered part of the equation which takes the maximum hole size, twice the annular ring requirement, and an appropriate manufacturing allowance.

The land pattern descriptions contained herein take into account these design recommendations and use the same principle to develop the through-hole component land patterns. Thus once the component lead configuration has been determined in addition to the variation to that spacing (lead extension, reforming of leads, etc.) the hole size is based on the hole to lead relationship shown in IPC-2222. This concept also has a variation based on the three complexity levels previously established.

The final concepts include making sure that the fabrication allowance when added to the previously defined dimensions can accommodate the hole, and solder joint requirements and thus determine the maximum boundary of the land pattern or component body dimension, whichever is greater.

Although the manufacturing allowance considers hole location and feature (land) location tolerances, copper plating, etch factor and material movement, there may sometimes be a need for the manufacturer to change the hole location by some minor variation in order to obtain the best land to hole relationship. Such tailoring of the X and Y location is considered normal manufacturing practices and in most instances does not impact the automated assembly conditions, provided that sufficient clearance between lead and hole diameters has been established. In addition, caution is recommended when converting imperial (inch) based dimensions to SI (metric) or vice-versa as the round-off factors have been known to impact the relationships between the mounting platform (holes and lands) and the assembly equipment tolerance capability.

3.1.4 Assembly Tolerancing Another part of the equation is the assembly variation. This variation represents the location of the component in relation to its true position as defined by the design. The term diameter of true position (DTP) is used to describe this variation and is a single number that can be used in any dimensional tolerance analysis. Since many manufacturing services prefer to build assemblies in pallet format, there is often more than one PB assembly contained within the pallet, either in an array format or in a random positioning of the assemblies. The location of components is described within the design data by the centroid of the component location in relationship to the point of origin of the assembly which is related to the point of origin of the pallet.

A major condition for component assembly is the final location of each land pattern, be it through-hole or surface mounting. This is particularly true for multiple-leaded components that must be considered in land pattern design, including their lead pitch and pin location accuracy. The pitch describes the basic dimension of the spacing of one component lead termination to its adjacent counterpart(s). No tolerance is assigned to pitch in the through-hole dimensioning concept. Differences in lead form and location are included in the hole dimensions used to accommodate the lead, however PB fabrication modifications are not taken into account and automated assembly equipment may need to be reprogrammed to ensure that the component position is understood by the assembly insertion machine. The use of local fiducials may help in re-orienting the x-y location.

3.1.5 Dimension and Tolerance Analysis In analysing the design of a component/land pattern system, several things come into play, including the size and position tolerances of the component lead, the tolerances of the land pattern, and the placement accuracy of the man/machine to center the part to the land pattern. The result is the land area available for a solder joint that provides a proper fill of the through-hole with solder and good wetting top to bottom. Component holes are usually plated and the MMC of the hole (when the plated-through hole is at its minimum size) must accommodate the lead diameter of the through-hole component. All dimensions and tolerances consider the hole as a supported (plated) with the exception of single-sided PBs which have only have lands on the side opposite (secondary) the component placement location (primary side).

For the tolerance analysis the dimensions considered for the lead to hole relationship come with an assumption that the end product hole diameter is a plated-through hole. Thus, the drilled hole diameter is somewhat larger in order to allow for plating within the hole wall. Because of multilayer internal padstack requirements, the drilled hole diameter is used as determining the minimum annular ring and thus the relationship between the land and lead diameter have been compensated by adding 0.1 mm to the hole clearance requirement in order to accommodate the plating of the through-hole. The land size therefore considers all the features that make up the land to hole relationship. Since the through-hole land requirements are based on multilayer technology, if a single side PB is used, the hole size will be a little larger. However, since the requirements for attachment require a lead clinch, the concepts used in this standard can work for both plated and non-plated hole characteristics.

In the event that a non-plated hole is used to attach a component lead which cannot be bent, the clearance between the lead and the hole are very critical and may need fine tuning in order to reduce the amount of excess room for the solder attachment. In this instance the hole to lead relationship is reduced to a minimum clearance of 0.015 mm between the hole diameter and the maximum lead diameter. The land pattern concepts provided in this standard **shall** have the hole size reduced, however it is recommended that the original land size be maintained in order to provide for a reliable solder joint formation.

If the requirement is for a condition of a through-hole component that is intended to be reflow soldered using intrusive reflow soldering techniques, the hole clearance relationship should also be reduced in order to have the solder flow into the plated-through hole and form a proper solder joint. In this instance the minimum clearance between the lead diameter and the finished plated-through hole diameter should also be reduced to a clearance of 0.015 mm between the maximum lead and the minimum internal diameter of the plated-through hole.

3.1.5.1 Tolerance and Solder Joint Analysis The following tolerance concepts are used to determine the land patterns for electronic components. These concepts reflect the tolerances on the component, the tolerances on the land pattern (on the interconnecting substrate), and the accuracy of the equipment used for placing components.

Solder joint minimums are based on the lead diameter and the clearance between the lead and the inside barrel of the hole. Lands fully circumscribe the hole diameter no matter their shape. This standard considers the minimum annular ring as the

minimum amount of copper (at the narrowest point) between the edge of the hole and the edge of the land after plating of the finished hole.

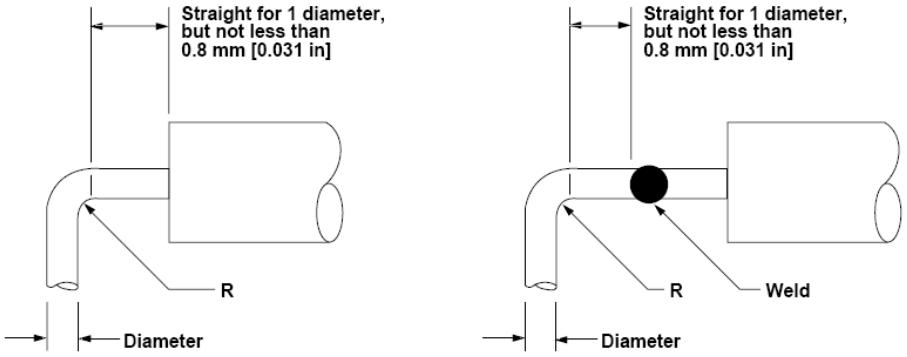
Land shapes may be extended in one or more directions to accommodate a more robust solder joint and thus have additional material available beyond the minimum annular ring in order to increase solder attachment capability. In these instances the land description may use teardrop or land elongation concepts.

The courtyard excess is added to the maximum dimension that the land pattern or component occupies. The courtyard excess number is added to each side of the dimension in question. It is intended that this addition provides sufficient room for electrical and physical clearance between components and/or land patterns.

The IPC-7251 land pattern libraries included within the IPC Land Pattern Viewer provide an analysis of tolerance assumptions and resultant solder joints based on the finished land pattern dimensions. Tolerances for component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration. These tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication and placement accuracy.

The dimensions for minimum solder fillets have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the IPC Land Pattern Viewer usually provide for a positive solder fillet. Nevertheless, if the user of any of the three land pattern geometry variations desires a more robust process condition for placement and soldering equipment, individual elements of the analysis may be changed to new and desired dimensional conditions. This includes component, PB or placement accuracy spread, as well as minimum solder joint or land to hole relationships. In addition, this standard recognizes the need to have different goals for the solder fillet or land attachment conditions.

Table 3-1 through Table 3-9 indicate the principles used for the three goals established by this standard. The tables reflect maximum, nominal and least material conditions for the land/hole solder attachment used to develop land patterns for through hole mounting of various leads of components. Unless otherwise indicated, the IPC-7251 identifies all three goals as Levels A, B, or C. Table 3-1 through Table 3-9 provide lead extensions from the body seal or lead weld and their associated bend radii as shown in Figure 3-5.



Note: Measurement shall be made from the end of the part. (The end of the part is defined to include any coating meniscus, solder seal, solder or weld bead, or any other extension.)

The span for components mounted with a conventional lead form is 0.8 mm [0.031 in] minimum, and 33 mm [1.30 in] maximum.

Maximum Lead Diameter	Minimum Radius (R)
Up to 0.8 mm [0.031 in]	1 diameter
From 0.8 mm [0.031 in] to 1.2 mm [0.0472 in]	1.5 diameters
Larger than 1.2 mm [0.0472 in]	2 diameters

Figure 3-5 Minimum Bend Radii for Axial Leaded Components

Table 3-1 Axial Leaded Components (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	0.25	0.2	0.15	Max Lead dia. plus value
Int. & Ext. Annular ring Excess (added to hole dia.)	0.50	0.35	0.30	Includes min. manufacturing allowance
Anti Pad Excess (added to hole dia.)	1.00	0.70	0.50	Includes min. manufacturing allowance
Lead Extension Max Lead Dia. 0.2 to 0.8	Straight for 1.2 plus 1 diameter bend radius	Straight for 1.0 plus 1 diameter bend radius	Straight for 0.8 plus 1 diameter bend radius	Minimum Component lead extension per side from body or weld
Lead Extension Max Lead Dia. 0.85 to 1.20	Straight for 2.2 lead diameters plus 1.5 bend radius	Straight for 1.8 lead diameters plus 1.5 bend radius	Straight for 1.5 lead diameters plus 1.5 bend radius	
Lead Extension Max Lead Dia. > 1.25	Straight for 2.8 lead diameters plus 2.0 bend radius	Straight for 2.4 lead diameters plus 2.0 bend radius	Straight for 2.0 lead diameters plus 2.0 bend radius	
Courtyard Excess from Component body or lands	0.5	0.25	0.1	Which ever is greater
Courtyard Round-off factor	Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.			Always round up
Axial Leaded Resistors (Round and Square) are described in 8.1.1 and 8.1.2. See Figure 3-6.				
Axial Leaded Capacitors (Non-Polarized, Polarized) are described in 8.1.3. See Figure 3-6				
Axial Leaded Diodes (Square, Oval, Round) are described in 8.1.4				
Axial Leaded Inductors (Square, Oval, Round) are described in 8.1.5				
Courtyard Determination Example				

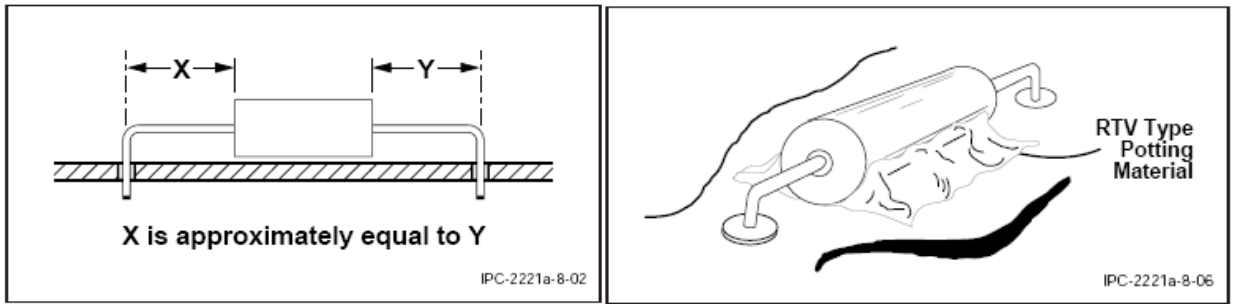


Figure 3-6 Axial Leaded Component

Table 3-2 Axial Leaded Parts Perpendicular Part Mounting, (Round and Square) (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	0.25	0.2	0.15	Max Lead dia. plus value
Int. & Ext. Annular ring Excess (added to hole dia.)	0.50	0.35	0.30	Includes min. manufacturing allowance
Anti Pad Excess (added to hole dia.)	1.00	0.70	0.50	Includes min. manufacturing allowance
Minimum Land Pitch	½ body + (H + 0.30) + 0.4	½ body + (H + 0.30) + 0.3	½ body + (H + 0.30) + 0.2	Electrical clearance between component body and land
Courtyard Excess from Component body or lands	0.5	0.25	0.1	Which ever is greater

Courtyard Round-off factor	**Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.**	**Always round up**
Axial Leaded Resistors, Perpendicular Part Mounting (Round and Square) are described in 8.1.1 and 8.1.2. See Figure 3-7.		
Axial Leaded Capacitors, Perpendicular Part Mounting (Non-Polarized, Polarized) are described in 8.1.3. See Figure 3-7.		
Courtyard Determination Example		

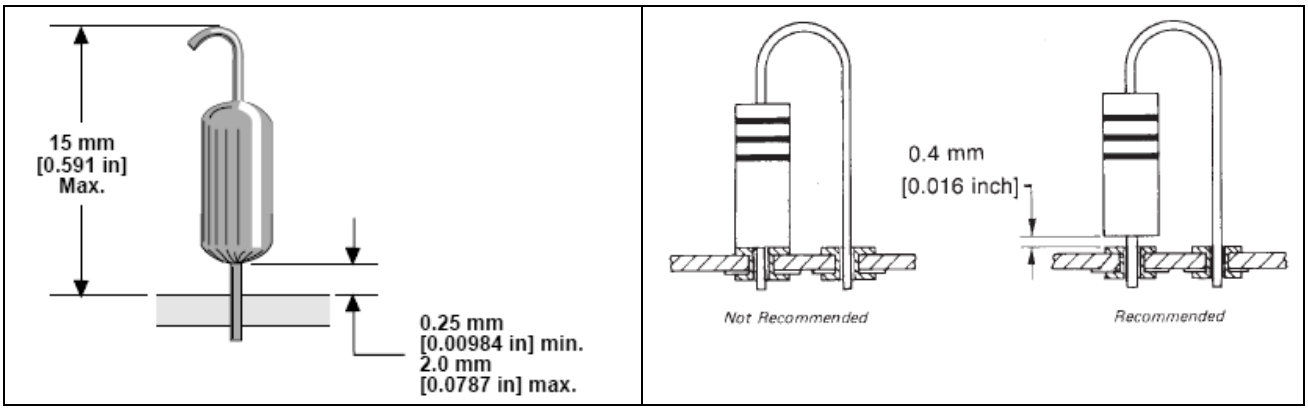
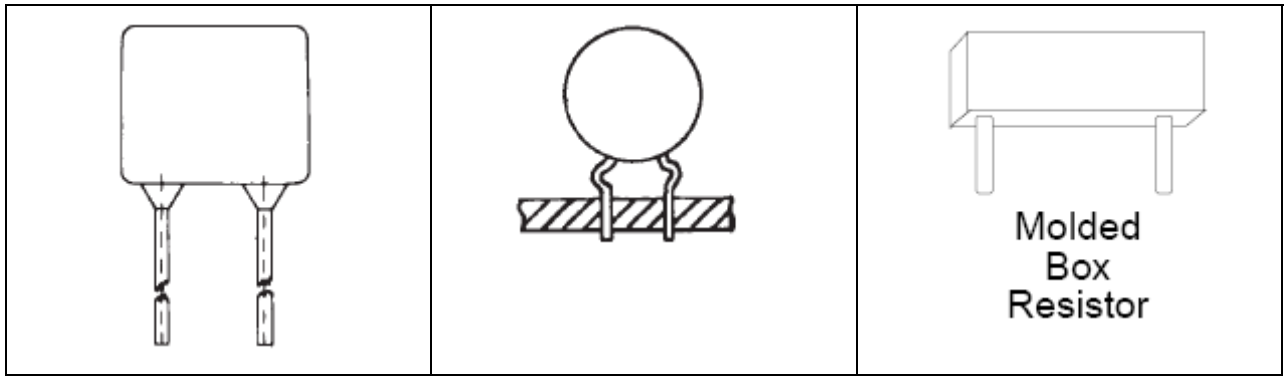


Figure 3-7 Axial Leaded Parts, Perpendicular Part Mounting

Table 3-3 Radial Leaded Parts Perpendicular Part Mounting, (Round, Square and Oval) (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	**0.25**	**0.2**	**0.15**	**Max Lead dia. plus value**
Int. & Ext. Annular ring Excess (added to hole dia.)	**0.50**	**0.35**	**0.30**	**Includes min. manufacturing allowance**
Anti Pad Excess (added to hole dia.)	**1.00**	**0.70**	**0.50**	**Includes min. manufacturing allowance**
Minimum Lead Spreading	**1.0 added to pitch**	**0.5 added to pitch**	**Not applicable**	**When leads can be bend outward**
Courtyard Excess from Component body and/or lands (which ever is greater)	**0.5**	**0.25**	**0.1**	**Courtyard contours to shape of component body and/or lands**
Courtyard Round-off factor	**Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.**			**Always round up**
Radial Leaded Capacitors Perpendicular Part Mounting, (Round, Square and Oval) are described in 8.2.1. See Figure 3-8.				
Courtyard Determination Example				



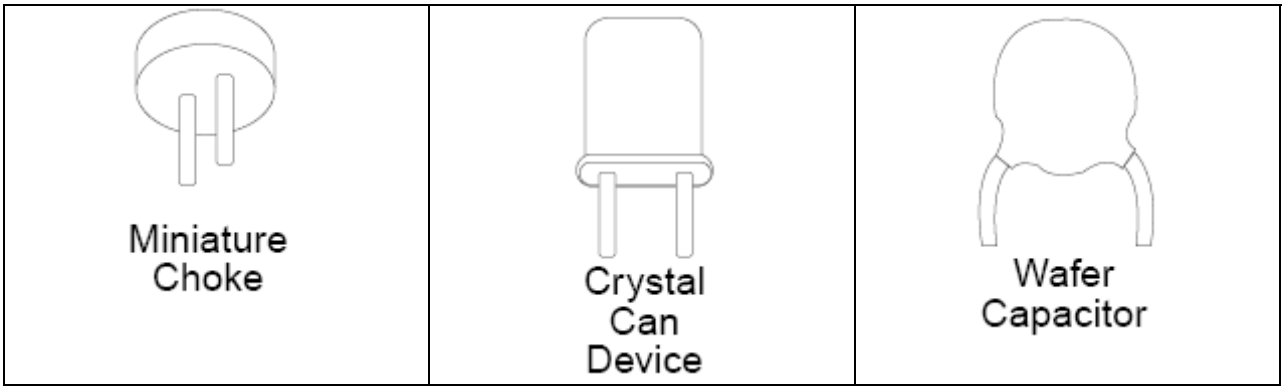


Figure 3-8 Radial Leaded Parts Perpendicular Part Mounting, (Round and Square)

Table 3-4 Single inline Package Resistor Network (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	0.25	0.2	0.15	Max Lead dia. plus value
Int. & Ext. Annular ring Excess (added to hole dia.)	0.50	0.35	0.30	Includes min. manufacturing allowance
Anti Pad Excess (added to hole dia.)	1.00	0.70	0.50	Includes min. manufacturing allowance
Courtyard Excess from Component body and/or lands	0.5	0.25	0.1	Which ever is greater
Courtyard Round-off factor	Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.			Always round up
Single inline Package Resistor Networks are described in section 14. See Figure 3-8.				
Courtyard Determination Example				

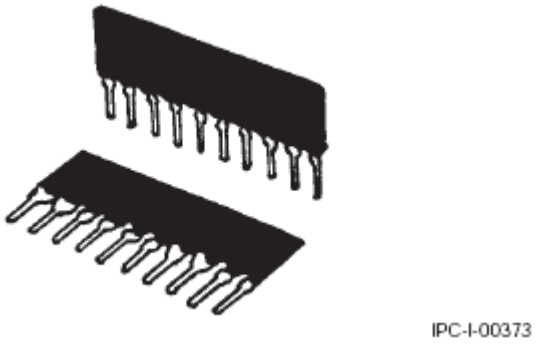


Figure 3-9 Single inline Package Resistor Network

Table 3-5 Dual In-Line Packages (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	0.25	0.2	0.15	Max Lead dia. plus value
Int. & Ext. Annular ring Excess (added to hole dia.)	0.50	0.35	0.30	Includes min. manufacturing allowance
Anti Pad Excess (added to hole dia.)	1.00	0.70	0.50	Includes min. manufacturing allowance
Courtyard Excess from Component body and/or lands	0.5	0.25	0.1	Which ever is greater
Courtyard Round-off factor	Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.			Always round up

Dual In-Line IC Packages are described in 9.1. See Figure 3-10.
Dual In-Line Package Resistor Networks are described in 9.2
Courtyard Determination Example

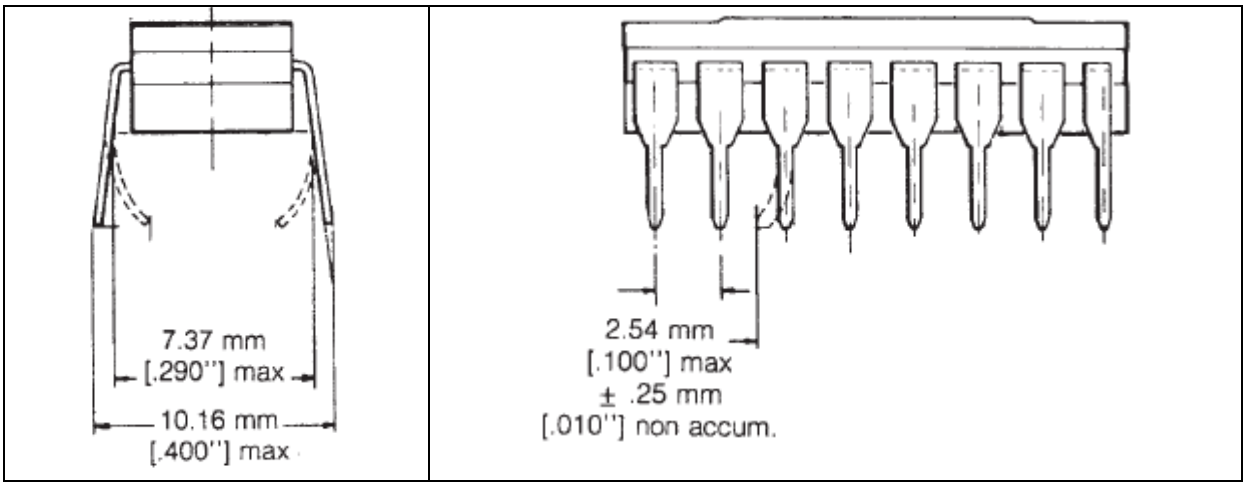


Figure 3-10 Dual In-Line Packages

Table 3-6 Dual In-Line Sockets (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	0.25	0.2	0.15	Max Lead dia. plus value
Int. & Ext. Annular ring Excess (added to hole dia.)	0.50	0.35	0.30	Includes min. manufacturing allowance
Anti Pad Excess (added to hole dia.)	1.00	0.70	0.50	Includes min. manufacturing allowance
Courtyard Excess from Component body and/or lands	0.5	0.25	0.1	Which ever is greater
Courtyard Round-off factor	Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.			Always round up
Dual In-Line Sockets are described in 9.3. See Figure 3-11.				
Courtyard Determination Example				

Figure 3-11 Dual In-Line Sockets (Need Figure)

Table 3-7 Three Leaded Parts, Perpendicular Part Mounting (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	0.25	0.2	0.15	Max Lead dia. Or lead dimple plus value
Int. & Ext. Annular ring Excess (added to hole dia.)	0.50	0.35	0.30	Includes min. manufacturing allowance
Anti Pad Excess (added to hole dia.)	1.00	0.70	0.50	Includes min. manufacturing allowance
Minimum Lead Spreading	1.0 added to pitch	0.5 added to pitch	Not applicable	When leads can be bend outward
Courtyard Excess from Component body and/or lands (which ever is greater)	0.5	0.25	0.1	Courtyard contours to shape of component body and/or lands
Courtyard Round-off factor	Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.			Always round up

TO 220 Transistors are described in 10.1. See Figure 3-12.
TO 92 Transistors are described in 10.2. See Figure 3-12.
TO 5 Transistors are described in 10.3. See Figure 3-12.
Courtyard Determination Example

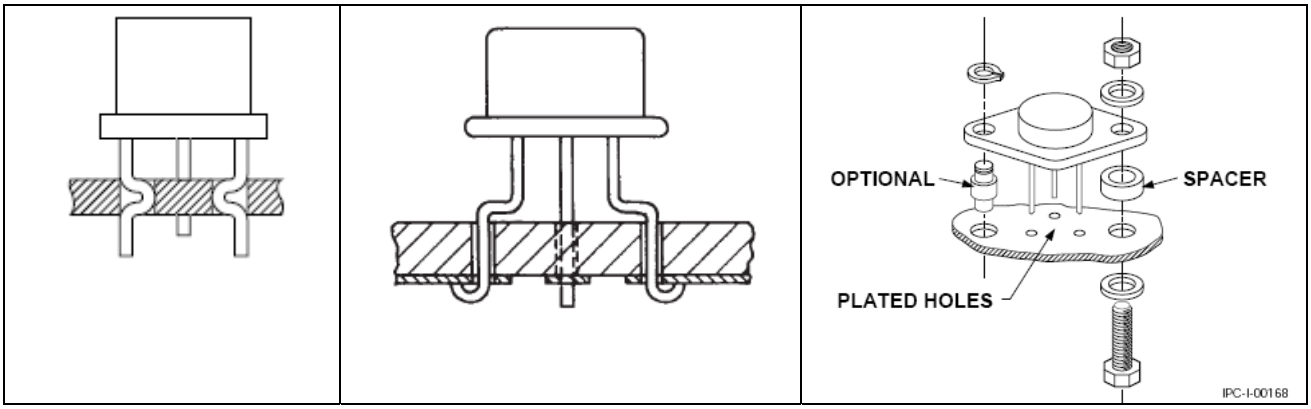


Figure 3-12 Transistors, Perpendicular Part Mounting

Table 3-8 Three Leaded Parts, Horizontal Part Mounting (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	0.25	0.2	0.15	Max Lead dia. Or lead dimple plus value
Int. & Ext. Annular ring Excess (added to hole dia.)	0.50	0.35	0.30	Includes min. manufacturing allowance
Anti Pad Excess (added to hole dia.)	1.00	0.70	0.50	Includes min. manufacturing allowance
Minimum Lead Spreading	1.0 added to pitch	0.5 added to pitch	Not applicable	When leads can be bend outward
Courtyard Excess from Component body and/or lands (which ever is greater)	0.5	0.25	0.1	Courtyard contours to shape of component body and/or lands
Courtyard Round-off factor	Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.			Always round up
TO 3 Power Transistors, Horizontal Part Mounting, are described in 10.4. See Figure 3-13.				
Courtyard Determination Example				

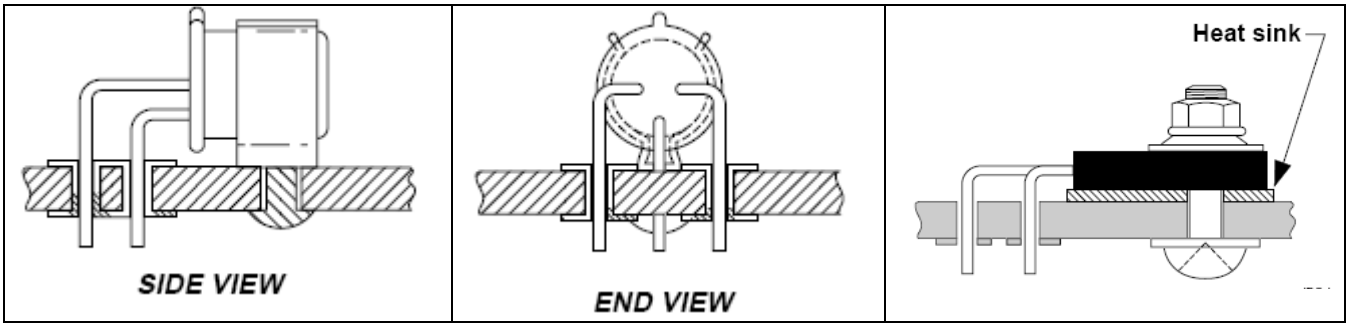


Figure 3-13 Transistor, Horizontal Part Mounting

Table 3-9 Multiple Leaded Semiconductors (unit: mm)

Joint Characteristics	Maximum Level A	Nominal Level B	Least Level C	Comments
Hole Diameter Factor	0.25	0.2	0.15	Max Lead dia. plus value
Int. & Ext. Annular ring Excess (added to hole dia.)	0.50	0.35	0.30	Includes min. manufacturing allowance
Anti Pad Excess (added to hole dia.)	1.00	0.70	0.50	Includes min. manufacturing allowance
Courtyard Excess from Component body and/or lands	0.5	0.25	0.1	Which ever is greater
Courtyard Round-off factor	Round up to the nearest even two place decimal, i.e., 1.00, 1.10, 1.20, 1.30 etc.			Always round up
Pin Grid Arrays are described in 11.1. See Figure 3-14.				
Courtyard Determination Example				

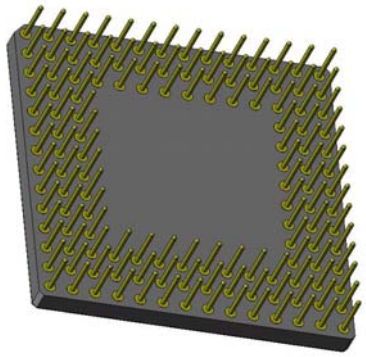


Figure 3-14 Pin Grid Array

3.1.5.2 Component Dimensions Illustrations of component dimensions in the IPC Land Pattern Viewer program are accompanied by a table of figures for each of the different part numbers, as taken from multinational component standards organizations. The standards organizations provide many more dimensions to define the requirements for manufacturing the specific components in a family class; only those dimensions that are necessary for land pattern development are repeated within the IPC Land Pattern Viewer program. At times, the component tolerances or component gauge requirements do not necessarily reflect the exact tolerance on a manufacturer's data sheet. Component dimensions are provided according to the concepts of maximum and least materials condition (MMC and LMC). Both conditions are presented in the IPC Land Pattern Viewer program. The component manufacturers may not always dimension their components in accordance with the limits shown in the IPC Land Pattern Viewer program. However, these limits may be used as criteria for go/no-go acceptance of the component.

Dimensions that have had their tolerance condition altered are so indicated in the IPC Land Pattern Viewer program. Parts that are available with shape characteristics or tolerance limits that fall outside the recommended norms require land patterns that must be altered slightly from those presented.

Users of these specialized parts are encouraged to develop their own land patterns which then become unique to a specific component vendor part. A dimensioning system with specific equations has been provided to facilitate unique land pattern development or enhance process usage.

3.1.5.3 Land Pattern Dimensions Land pattern dimensions are provided in the IPC Land Pattern Viewer software program according to the concepts of maximum material conditions (MMC).

Sometimes a dimension is presented as a minimum distance. This occurs when defining a space(s) that exists between lands at MMC. The PB manufacturer may not always inspect the PB in accordance with the limit concepts shown in the table. However, these limits may be used as the criteria for go/no-go acceptance of the PB land pattern. The dimensions shown in the IPC Land Pattern Viewer program are based on Table 3-1 through Table 3-9. The maximum material condition for each land pattern analysis level describes the most robust joint for that level land pattern.

3.1.5.4 Through-Hole Courtyard Determination The courtyard of any land pattern is the smallest area that provides a minimum electrical and mechanical clearance of both the component maximum boundary extremities and/or the land pattern maximum boundary extremities. The intent of the courtyard is to aid the designer in determining the minimum area occupied by the combination of component and land pattern. The information provided in Table 3-1 through Table 3-9 is intended to relate to those excesses that should be added to the maximum dimension to derive the appropriate courtyard condition.

As an example, if a component was the major determining factor of the boundary condition, it would have the excess added to the dimensions. The same holds true for a land pattern that has the greater extremities. If either dimension were 14.5 mm, and the excess from Table 3-1 through Table 3-9 indicated an excess of 0.8 mm, the resulting courtyard would theoretically be 16.1 mm. The tables further define a round-up feature. If the round-up were recommended as being to the nearest 0.5 mm, the courtyard would become 16.5 mm.

It should be noted that 16.5 mm is a number that, when divided by 2 to obtain the component centroid, provides 2 decimal places to the right of the number. It therefore may be appropriate to keep this number in an even approximation such as 16.6 mm. This would provide 8.3 mm to either side of the center of the component to help designers position the component in relation to some grid or placement algorithm.

When manufacturing allowance must be considered in the design process the courtyard represents the starting point of the minimum area needed for the component and the land pattern. Manufacturing, assembly and testing representatives should assist in determining the additional room needed to accommodate placement, testing, modification and repair. This manufacturing allowance is usually dependent on the density and complexity of the product, and is not defined in this document. The manufacturing allowance is determined by application and manufacturing process requirements (see Figure 3-15).

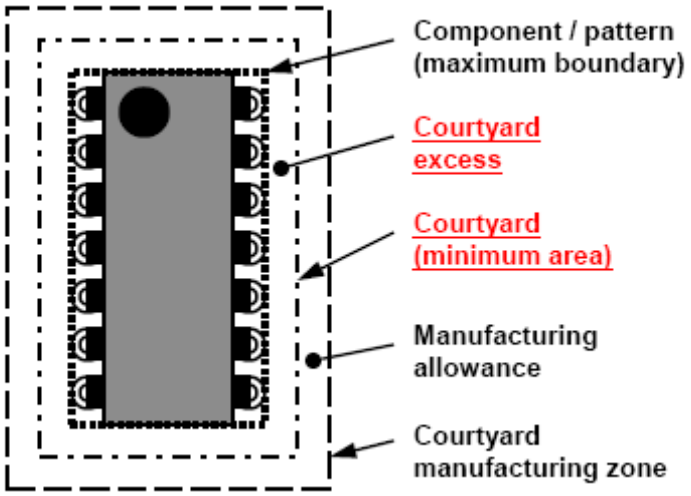


Figure 3-15 Through-Hole Courtyard Boundary Area Condition

3.1.5.5 Pad Stack Naming Convention The padstack consists of combinations of letters and numbers that represent shape, or dimensions of lands on different layers of PBs or documentation. The name of the padstack needs to represent all the various combinations. These are used in combination with the land pattern conventions defined herein according to the rules established in the IPC-2220 series of PB design standards.

The first part of the padstack convention consists of a land shape. There are six basic land shape identifiers.

Note: All alphabetical characters are “lower case”. This helps discriminate numeric values.

Basic Land Shape Letters

c = Circular
s = Square
r = Rectangle
b = Oblong
u = Contour (Irregular Shape)
d = D Shape (Square on one end and Circular on the other end)

Note: An oval padstack is considered the same as an oblong padstack. This document uses the term “oblong”.

Padstack Defaults

- Solder Mask is 1:1 scale of the land size
- Paste Mask is 1:1 scale of the land size
- The Assembly Layer land is 1:1 scale of the land size
- Inner Layer Land is the same shape as the outer layer land
- The Primary and Secondary lands are the same size
- The inner layer land shapes are Circular
- Vias are Circular
- Thermals have 4 spokes
- Mounting Holes are Circular

Note: Every PB fabricator's ability to register solder mask is different. The 1:1 covers the variation, provided that PBs are fabricated to industry specifications such as IPC-6012 which state that there cannot be mis-registration of the solder mask.

Illegal characters that cannot be used (Microsoft® requirement) include " " , ; : / \ [ ] ( ) . { } * & % # $! @ ^ =

Examples utilizing the padstack naming convention (all values are in metric units)
Note: Every number goes two places to the right and as many as needed to the left of the decimal
Examples: 1150 = 11.50 mm or 11500 µm, 150 = 1.50 mm or 1500 µm, 15 = 0.15 mm or 150 µm

c150h90 where C denotes a Circular land with a 1.50 diameter and H denotes a hole size of 0.90

v50h25 where a V denotes a via with a 0.50 land (default Circular land) and H denotes a 0.25 hole

s150h90 where S denotes a 1.50 Square land and H denotes a hole size of 0.90

s350 where S denotes a square SMT land size of 3.50

r200_100 where R denotes a Rectangular SMT land 2.00 land length X 1.00 land width

b300_150 where B denotes a SMT Oblong land size of 3.00 X 1.50

b400_200h100 where R denotes an Oblong land size of 4.00 length X 2.00 width and 1.00 hole

d300_150 where D denotes land with one circular end and one square end (looks like a D) 3.00 X 1.50

v30h15l1-3 where V denotes a 0.30 blind via with 0.15 Hole; 1 is the starting layer, 3 is the end layer

v30h15l3-6 where V denotes a 0.30 buried via with 0.15 Hole; 3 is the starting layer, 6 is the end layer

It is assumed that the padstack has the same value as the mounted layer size and shape for:

- Inner Layer
- Opposite Side
- Solder Mask
- Solder Paste
- Assembly Layers

It is also assumed that the "Plane Clearance" and "Thermal Relief" data follows the through-hole convention guidelines defined in the IPC-2221 and IPC-2222 standards.

3.1.5.5.1 Pad Stack Naming Convention Modifiers The padstack naming convention includes Modifiers that are used when padstack features are different than the defaults. These are the "Variants" or "Modifiers" that go after the basic padstack naming convention.

These are used when the User needs to change the padstack default values either by a different dimension or a different shape. In instances where shapes are different this becomes a two letter code with the modifier first followed by the land shape letter:

n = Non-plated Hole
z = Inner Layer land dimension if different than the land on primary layer
x = Special modifier used alone or following other modifiers for lands on opposite side to primary layer land dimension
t = Thermal Relief; if different than the land convention that matches land on primary layer
m = Solder Mask if different than default 1:1 scale of land

p = Solder Paste if different than default 1:1 scale of land
a = Assembly surface land if different than default 1:1 scale of land
y = Plane Clearance is a different value than the default
o = Offset Land Origin

Shape change is the last letter in the string prior to the dimension.

3.1.5.5.2 Other Usages of The Padstack Naming Convention

USE of letter v: Vias can be named using the pad stack naming convention. Because most vias use lands that are circular in shape, the letter V will be used in place of the letter C in the padstack naming convention. If this is not true the modifiers can be added after the letter V to signify shape or dimensional changes to this default.

USE of letter w: Mounting holes can be named using the padstack naming convention. The letter W shall be used to define the mounting hole characteristics and any associated lands used for the surface lands (either plated or non-plated)

Examples of double character modifiers:

ts = Thermal Square; if different than the top side land shape and dimensions
tt = Thermal with 2 spokes
ttt = Thermal with 3 spokes
zs = Inner Layer Land Shape is Square (Note: The default is circular)
m0 = No Solder Mask
mxc = Solder Mask Opposite Side Circular
mx0 = Solder Mask Opposite Side No Solder Mask
xc = Opposite Side Circular
vs = Via with Square land
hn = Non-plated Hole

Modifier Examples:

s150h90zs150 = Square 1.50 land with 0.90 Hole with 1.50 inner (Z) Layer Square land
vS50h25 where VS denotes a 0.50 Square Via with a 0.25 Hole
v50h25xs70 where V is 0.50 Circular Via with 0.25 Hole and 0.70 Square land on opposite side

Examples of a padstack with circular land with hole using various modifiers

Note: The use of italics in the following examples are for denoting modifiers in this standard. These modifiers do not appear as italics in IPC-7x51 supporting software.

c150h90 = Default padstack with a 1.50 circular land with a 0.90 hole (no modifiers used)

c150h*n*90 = Default padstack with a 1.50 circular land with a 0.90 non-plated hole

c150h90z*140* = Inner layer land is smaller than external lands 1.40 or 0.10 smaller

c150h90z140x*170* = Opposite side land is larger than top side land 1.70 or 0.20 larger

c150h90z140X170*m165mX185* = Solder mask opening for top and bottom lands 0.15 larger for each

c150h90z140x170m165mX185*a200* = Assembly drawing land in 0.50 larger than 1.50 primary land

c150h90z140X170m165mx185a200*y300* = Plane clearance anti-pad diameter is 3.00

c150h90z140x170*m165mX85* = Solder mask encroachment on opposite land by 0.65 smaller

c150h90*m165* = adding a solder mask opening of 1.65 diameter or 0.15 larger than land

Examples of a padstack with Oblong land with Slotted Hole

Sample – **b** = Oblong Land Shape then "**X**" dimension (length) then Underscore **_** "**Y**" dimension (width)

b400_200h300_100 = Oblong land 4mm length X 2mm width with slotted hole size 3mm X 1mm

b400_200h*n*300_100 = Oblong land 4mm X 2mm with non-plated slotted hole size 3mm X 1mm

Examples of a SMT padstack land using various modifiers

b300_150 = Default padstack with a 3.00 length and 1.50 width land (no modifiers used)

b300*_150m330_180* = Solder Mask is 0.30 larger than the land

b300_150m330*_180p240_140* = Solder Paste is smaller by 0.10 width and 0.60 length

b300_150o-50 = Oblong Land 3.0mm X 1.5mm w/Offset Origin negative 0.5mm

r400_200pb430_230 = Rectangle SMT land 4.00 X 2.00 with an Oblong Solder Paste size of 4.30 X 2.30

Example of a Mounting Hole

w700h400z520m720 = This is a Plated Through Mounting hole for a #6-32 screw using a 4.00 diameter hole and having a circular 7.00 land on the primary and secondary side of the PB, with a solder mask clearance that is 0.20 larger than the 7.20 land. The internal lands are smaller that the external and are also circular 5.20 in diameter.

w700h*n*400z520m720 = Non-plated version

3.1.5.6 Land Pattern Naming Convention The land pattern naming convention uses component dimensions to derive the land pattern name. The first 3 – 6 characters in the land pattern name describe the component family. The first number in the land pattern name refers to the lead spacing or hole to hole location to insert the component lead. All numbers that follow the lead spacing are component dimensions.

These characters are used as component body identifiers that precede the value and this is the priority order of the component body identifiers:

P = Pitch for components with more than two leads
W = Maximum Lead Width (or Component Lead Diameter)
L = Body Length for horizontal mounting
D = Body Diameter for round component body
T = Body Thickness for rectangular component body
H = Height for vertically mounted components
Q = Pin Quantity for components with more than two leads
R = Number of Rows for connectors
A, **B** & **C** = the producibility level as defined in the IPC-2221 and IPC-2222

Notes:

1) All component body values are in millimeters and go two places to the right of the decimal point and no leading zeros.
2) All producibility levels used in the examples are "**B**".
3) All dimensions are in Metric Units
4) All lead span and height numbers go two places past the decimal point and "include" trailing zeros
5) All lead span and body sizes go two place before the decimal point and "remove" leading zeros
6) All chip component body sizes are one place to each side of the decimal point
7) Pitch values are two places to the right & left of decimal point with no leading zeros but include trailing zeros

Component, Category	**Land Pattern Name**

Capacitors, Non Polarized Axial Diameter Horizontal Mounting..... **CAPAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example: CAPAD800W52L600D150B
Capacitors, Non Polarized Axial Diameter; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50

Capacitors, Non Polarized Axial Rectangular ..... **CAPAR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height
Example: CAPAR800W52L600T50H70B
Capacitors, Non Polarized Axial; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Thickness 0.50; Body Height 0.70

Capacitors, Non Polarized Axial Diameter Vertical Mounting ..... **CAPADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example: CAPADV300W52L600D150B
Capacitors, Non Polarized Axial; Lead Spacing 3.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50mm

Capacitors, Non Polarized Axial Rect. Vert. Mtg. ..... **CAPARV** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body Thickness + **H** Body Height
Example: CAPARV300W52L600T50H70B
Capacitors, Non Polarized Axial Rect. Vertical; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Thickness 0.50; Body Height 0.70

Capacitors, Non Polarized Radial Diameter ..... **CAPRD** + Lead Spacing + **W** Lead Width + **D** Body Diameter + **H** Body Height
Example: CAPRD200W52D300H550B
Capacitors, Non Polarized Radial Diameter; lead spacing 2.00; lead width 0.52; Body Diameter 3.00; Height 5.50

Capacitors, Non Polarized Radial Rectangular ..... **CAPRR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height
Example: CAPRR200W52L50T70H550B
Capacitors, Non Polarized Radial Rectangular; lead spacing 2.00; lead width 0.52; Body Length 0.50; Body thickness 0.70; Height 5.50

Capacitors, Non Polarized Radial Disk Button ..... **CAPRB** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height
Example: CAPRB200W52L50T70H550B
Capacitors, Non Polarized Radial Rectangular; lead spacing 2.00; lead width 0.52; Body Length 0.50; Body thickness 0.70; Height 5.50

Capacitors, Polarized Axial Diameter Horizontal Mounting ..... **CAPPAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example: CAPPAD800W52L600D150B
Capacitors, Polarized Axial Diameter; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50

Capacitor, Polarized Radial Diameter ..... **CAPPRD** + Lead Spacing + **W** Lead Width + **D** Body Diameter + **H** Body Height
Example: CAPPRD200W52D300H550B
Capacitors, Polarized Radial Diameter; lead spacing 2.00; lead width 0.52; Body Diameter 3.00; Height 5.50

Diodes, Axial Diameter Horizontal Mounting ..... **DIOAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example: DIOAD800W52L600D150B
Diodes, Non Polarized Axial Diameter; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50

Diodes, Axial Diameter Vertical Mounting ..... **DIOADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example: DIOADV300W52L600D150B
Diodes, Non Polarized Axial; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50

Dual-In-Line Packages ..... **DIP** + Lead Span + **W** Lead Width + **P** Pin Pitch + **L** Body Length + **H** Component Height + **Q** Pin Qty
Example: DIP762W52P254L1905H508Q14B
Dual-In-Line Package: Lead Span 7.62; Lead Width 0.52; Pin Pitch 2.54; Body Length 19.05; Body Height 5.08; Pin Qty 14

Dual-In-Line Sockets ..... **DIPS** + Lead Span + **W** Lead Width + **P** Pin Pitch + **L** Body Length + **H** Component Height + **Q** Pin Qty
Example: DIPS762W52P254L1905H508Q14B
Dual-In-Line Package Socket: Lead Span 7.62; Lead Width 0.52; Pin Pitch 2.54; Body Length 19.05; Body Height 5.08; Pin Qty 14

Headers, Vertical ..... **HDRV** + Lead Span + **W** Lead Width + **P** Pin Pitch + **R** Pins per Row + **L** Body Length + **T** Body Thickness + **H** Component Height
Example: HDRV200W52P200R2L4400T400H900B
Header, Vertical: Lead Span 2.00; Lead Width 0.52; Pin Pitch 2.00; 2 Rows; Body Length 44.00; Body Thickness 4.00; Body Height 9.00

Headers, Right Angle . **HDRRA** + Lead Span + **W** Lead Width + **P** Pin Pitch + **R** Pins per Row + **L** Body Length + **T** Body Thickness + **H** Component Height
Example: HDRRA200W52P200R2L4400T400H900B
Header, Vertical: Lead Span 2.00; Lead Width 0.52; Pin Pitch 2.00; 2 Rows; Body Length 44.00; Body Thickness 4.00; Body Height 9.00

Inductors, Axial Diameter Horizontal Mounting ..... **INDAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example: INDAD800W52L600D150B
Inductors, Axial Diameter; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50

Inductors, Axial Diameter Vertical Mounting ..... **INDADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example: INDADV300W52L600D150B
Inductors, Axial Diameter Vertical Mounting; Lead Spacing 3.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50

Jumpers, Wire ..... **JUMP** + Lead Spacing + **W** Lead Width
Example: JUMP500W52B
Jumper; Lead Spacing 5.00; Lead Width 0.52

Mounting Holes Plated With Support Pad ..... **MTGP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size
Example: MTGP700H400Z520
This is a Mounting hole for a #6-32 screw using a circular 7.00 land on the primary and secondary side of the PB, a 4.00 diameter hole with the internal lands are smaller that the external and are also circular 5.20 in diameter.

Mounting Holes Non-Plated With Support Pad ..... **MTGNP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size
Example: MTGNP700H400Z520
This is a Mounting hole for a #6-32 screw using a circular 7.00 land on the primary and secondary side of the PB, a 4.00 diameter hole with the internal lands are smaller that the external and are also circular 5.20 in diameter.

Mounting Holes Non-Plated Without Support Pad ..... **MTGNP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size + **K** Keep-out Diameter
Example: MTGNP100H400Z520K700
This is a Mounting hole for a #6-32 screw using a circular 1mm land on the primary and secondary side of the PB, a 4.00 diameter hole with the internal lands are smaller that the external and are also circular 5.20 in diameter and a 7.00 diameter keep-out.

Mounting Holes Plated with 8 Vias ..... **MTGP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size + 8 Vias
Example: MTGP700H400Z520V8
This is a Mounting hole for a #6-32 screw using a circular 7mm land on the primary and secondary side of the PB, a 4mm diameter hole with the internal lands are smaller that the external and are also circular 5.2mm in diameter, with 8 vias.

Pin Grid Array's ..... **PGA** + Pin Qty + **P** Pitch + **C** Pin Columns + **R** Pin Rows + **L** Body Length **X** Body Width + **H** Component Height
Example: PGA84P254C10R10L2500X2500H300B
Pin Grid Array: Pin Qty 84; Pin Pitch 2.54; Columns 10; Rows 10; Body Length 25.00 X 25.00; Component Height 3.00

Resistors, Axial Diameter Horizontal Mounting ..... **RESAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example:: **RESAD800W52L600D150B**
Resistors, Axial Diameter; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50

Resistors, Axial Diameter Vertical Mounting .....**RESADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Example: RESADV300W52L600D150B
Resistors, Axial Diameter Vertical Mounting; Lead Spacing 3.00; Lead Width 0.52; Body Length 6.00; Body Diameter 1.50

Resistors, Axial Rectangular Horizontal Mounting..... **RESAR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height
Example: RESAR800W52L600T50H70B
Resistors, Axial Rectangular; Lead Spacing 8.00; Lead Width 0.52; Body Length 6.00; Body Thickness 0.50; Body Height 0.70

Test Points, Round Land .....**TP** + Lead Width
Example: TP52

Test Points, Square Land..... **TPS** + Lead Width
Example: TPS52

Test Points, Top Land Round & Bottom Land Square.....**TPRS** + Lead Width
Example: TPRS52

Wire .....**PAD** + Wire Width
Example: PAD52

Naming Convention Special Character Use for Land Patterns

The **_** (underscore) is the separator between pin Qty in Hidden & Deleted pin components

Suffix Naming Convention for Land Patterns

Common PTHT Land Pattern to Describe Environment Use (This is the last character in every name)

- **A** .....Most Material Condition (Level A)
- **B**.....Nominal Material Condition (Level B)
- **C** .....Least Material Condition (Level C)

The level of complexity is defined in a usage table and thus the lead diameter is used to associate the padstack with the component. If the user needs to modify the default padstack, it is recommended to modify the environment use letter by adding a unique number. i.e., B1, B2, B3, etc. It is recommended that the user who adopts this feature maintain a history archive that clearly identifies the padstack modifications associated with their unique numbering scheme such that future uses avoids duplication of padstack association with the land pattern name.

Reverse Pin Order

- **-20RB** .....20 pin part, Reverse Pin Order, Nominal Material Condition (Level B)

Hidden Pins

- **-20_24B** .....20 pin part in a 24 pin package. The pins are numbered 1 – 24 the hidden pins are skipped. The schematic symbol displays up to 24 pins.

Deleted Pins

- **-24_20B** .....20 pin part in a 24 pin package. The pins are numbered 1 – 20. The schematic symbol displays 20 pins.

Connectors (Miscellaneous Connector Libraries)

3M™ .....3M_Part Number
AGILENT™..... AGILENT_Part Number
AIRBORNE™ ..... AIRBORNE_Part Number
AMPHENOL™.....AMPHENOL_Part Number
AVX™.....AVX_Part Number
BERG™.....BERG_Part Number
BLOCKMASTER ELECTRONICS™ .....BLOCKMASTER_Part Number
CUI-STACK™..... CUI-STACK_Part Number
E.F. JOHNSON™..... JOHNSON_Part Number
FCI ELECTRONICS™..... FCI_Part Number
FUJITSU™ ..... FUJITSU_Part Number
HIROSE™ ..... HIROSE_Part Number
ITT CANNON™ .....ITT_Part Number
JALCO™..... JALCO_Part Number

JWT™ ..... JWT_Part Number
JST™ ..... JST_Part Number
KEYSTONE™ ..... KEYSTONE_Part Number
KYCON™ ..... KYCON_Part Number
LEMO™ ..... LEMO_Part Number
MILL-MAX™ ..... MILL-MAX_Part Number
MOLEX™ ..... MOLEX_Part Number
NEUTRIK™ ..... NEUTRIK_Part Number
PHOENIX™ ..... PHOENIX_Part Number
PULSE™ ..... PULSE_Part Number
RIA™ ..... RIA_Part Number
SAMTEC™ ..... SAMTEC_Part Number
SIEMENS™ ..... SIEMENS_Part Number
SPEEDTECH™ ..... SPEEDTECH_Part Number
STEWART™ ..... STEWART_Part Number
SULLINS™ ..... SULLINS_Part Number
SWITCHCRAFT™ ..... SWITCHCRAFT_Part Number
TYCO™ ..... TYCO_Part Number
YAMAICHI™ ..... YAMAICHI_Part Number

3.2 Design Producibility As part of the planning cycle of a product's development, a concurrent engineering task group should be assembled to determine the criteria for each new design. During this planning phase, the product function and configuration is clearly defined and the assembly process options outlined. Product size, component types, projected volume and the level of manufacturing equipment available may affect process options.

Following the substrate development, the assembly will be evaluated for many of the fundamentals necessary to insure a successful assembly process. Specific areas addressed during the evaluation include:

a) Land pattern concepts
b) Component selection
c) Mounting substrate design
d) Assembly methods (manual, automated, equipment used, etc.)
e) Sequence of intermixed component insertion/placement
f) Method of test
g) Phototool or circuit image generation
h) Meeting minimum solder joint requirements
i) Stencil fixture requirements
j) Wave solder fixture requirements
k) Providing access for inspection
l) Providing access for rework and repair

3.2.1 Land Patterns The use of process proven land patterns for the solder attachment of through-hole and surface mount devices will provide a benchmark to evaluate solder joint quality. Land pattern geometry and spacing utilized for each component type must accommodate all physical variables including size, material, lead contact design and plating.

3.2.2 Standard Component Selection Whenever possible, devices should be selected from standard configurations. The standard components will be available from multiple sources and will usually be compatible with assembly processes. For those devices developed to meet specific applications, standard packaging is often available. Select a package type that will be similar in materials and plating of standard device types when possible.

3.2.3 Circuit Substrate Development Design the circuit substrate to minimize excessive costs. High component density applications often push the leading edge of substrate technology. In addition, the needs for using new solder alloys makes determining land pattern variations critical. Since the choices in this standard have provided three conditions, users are encouraged to determine the flow characteristics of their new soldering processes. The derived land patterns are based on a mathematical model which is transparent to the soldering process. Never the less, since the use of some lead-free solder alloys react differently than the traditional tin/lead solder, the optimized version of the land pattern should be selected. The conditions of component lead finish, land pattern surface finishes, solder alloy being used, and the solder deposition method or reflow profile are more significant for achieving a reliable solder joint than the land pattern dimensions. When estimating circuit density, allow for the greatest latitude in fabrication processes and tolerance variables. Before adopting extreme fine-line and utilizing small plated holes, understand the cost impact, yield, and long-term reliability of the product.

3.2.4 Assembly Considerations Manufacturing efficiency includes component insertion and placement. Within the constraints of circuit function, maintaining a consistent spacing between components and common orientation or direction of polarized devices can have an impact on all steps of the assembly process. In addition, when common orientation is maintained, machine programming is simplified and component verification, solder inspection and repair are simplified.

3.2.5 Provision for Automated Test Testability of the assembled circuit substrate must be planned well in advance. If component level In-Circuit Test (ICT) is necessary, one test probe contact area is required for each common node or net. Ideally, all probe contact lands are on one side, typically the secondary side (double sided test fixtures are significantly more expensive). Functional testing may also employ the same test nodes used for in-circuit test but will include all connectors that interface to cables and other assemblies.

3.2.6 Documentation Documentation used to fabricate the circuit substrate and assemble the product must be accurate and easy to understand. Details, specifications and notes will guide both the assembly processing and control the quality level of a product. Unique materials or special assembly instructions, such as moisture sensitivity and handling, should be included on the face of the detail drawings or in the documentation package.

3.3 Environmental Constraints

3.3.1 Moisture Sensitive Components Plastic encapsulated IC packages may be susceptible to absorbing moisture. The component manufacturer usually provides specialized packaging for these, and furnish instructions for use or maintaining those parts in a controlled storage environment. IPC/JEDEC-020 provides moisture sensitivity levels while IPC/JEDEC J-STD-033 provides proper handling and testing methods such as for moisture sensitivity.

3.3.2 End-Use Environment Considerations Compounds, materials and assembly processes should consider the products end-use environment. Table 3-22 provides information on how the end-use environment characteristics for nine basic environments. These conditions may be used to evaluate the characteristics of the solder joints for both surface mount and through-hole component attachment. The grain structure of the solder alloy is impacted by the cyclic conditions of the final assembly and evaluations of the solder joint may help establish the correct process and materials combinations to ensure reliable attachment properties.

3.4 Design Rules The PB design principles recommended in this standard consider current test and manufacturing capabilities for through-hole components. For surface mount components, see IPC-7351. Exceeding the limitation of these capabilities requires concurrence of all participants in the process including manufacturing, engineering and test technology. Involving test and manufacturing early in the design helps to move a quality product quickly into production.

Manufacturing engineering should be consulted regarding any components outside the scope of this document.

3.4.1 Component Spacing

3.4.1.1 Component Considerations The land pattern design and component spacing affect the reliability, manufacturability, testability and repairability of assemblies. A minimum inter-package spacing is required to satisfy all these manufacturing requirements. Maximum inter-package spacing is limited by several factors, such as available PB space, equipment, weight considerations, and circuit operating speed requirements. Some designs require that surface mount components be positioned as close to one another as possible.

3.4.1.2 Wave Solder Component Orientation On any PB assembly where through-hole and surface mount devices are to be wave soldered, the orientation of devices in respect to the solder wave can contribute to excessive solder process defects. Figure 3-16 shows the application of attaching surface mount and through-hole components using wave solder techniques. The preferred orientation compared in Figure 3-17 optimizes the solder process, minimizing solder bridging on the trailing or shadowed contacts as the assembly exits the solder wave. All polarized surface mount components should be placed in the same orientation when possible. The following additional conditions apply:

a) All passive components should be parallel to each other

b) The longer axis of SOICs and the longer axis of passive components shall be perpendicular to each other

c) The long axis of passive components shall be perpendicular to the direction of travel of the PB along the conveyer of the wave solder machine.

3.4.1.3 Component Insertion and Placement Similar types of components should be aligned on the PB in the same orientation for ease of component insertion, placement, inspection, and soldering. Also, similar component types should be grouped together whenever possible, with the net list or connectivity and circuit performance requirements ultimately driving the placements. In memory PBs, for example, all of the memory chips are placed in a clearly defined matrix with pin one orientation in the same direction for all components. This is a good design practice to carry out on logic designs where there are many similar component types with different logic functions in each package. On the other hand, analogue designs often require a large variety of component types making it understandably difficult to group similar components together. Regardless of whether the design is memory, general logic, or analog, it is recommended (when possible) that the orientation of pin 1 on all IC components is the same, provided that product performance or function is not compromised.

3.4.1.4 Grid-Based Component Positioning Component placement is generally more complex than PIH PBs for two reasons: higher component densities, and the ability to put components on both sides of the PB. In high component density designs the spacing between lands of different components are often less than 0.2 mm. Grid-based device placement may not be practical due to the large variety of component shapes.

Two effects created by random component arrangement are a loss of uniform grid-based test node accessibility and a loss of logical, predictable routing channels on all layers (possibly driving layer counts). In addition, the accepted international grid identified in IPC-1902 states that for new designs the grid should be 0.5 mm, with a further subdivision being 0.05 mm. One solution to the problem is to build CAD libraries with all component lands connected to vias on 0.5 mm centers (or greater, based on design) to be used for testing, routing, and rework ports.

It is easier to process a PB that has uniform component center-point spacing across the PB in both directions (see Figure 3-17).

3.4.2 Single-and Double-Sided PB Assembly The term single-sided PB assembly refers to components mounted or inserted on one side, and the term double-sided refers to components mounted or inserted on both sides of the PB. The double-sided PB assembly may require additional solder and assembly process steps and can increase manufacturing cost. Designers should concentrate on locating all components on the primary side of the PB whenever possible.

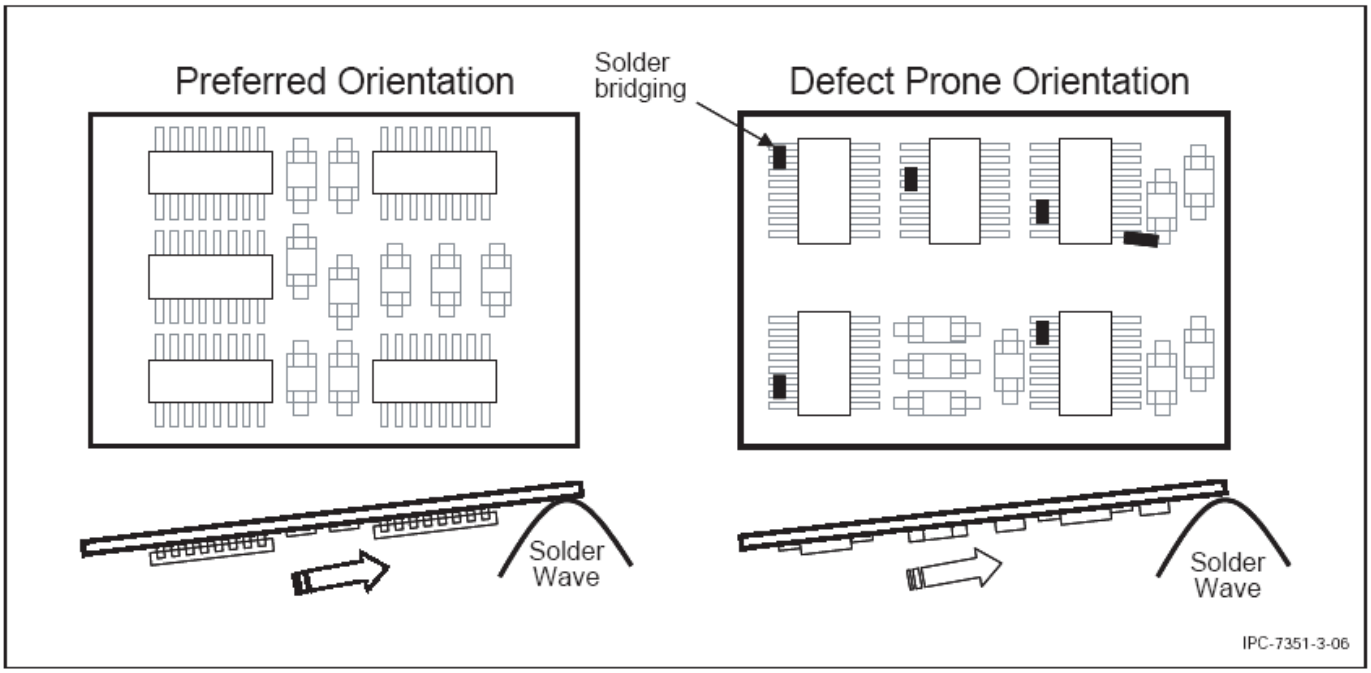


Figure 3-16 Component Orientation for Wave-Solder Applications

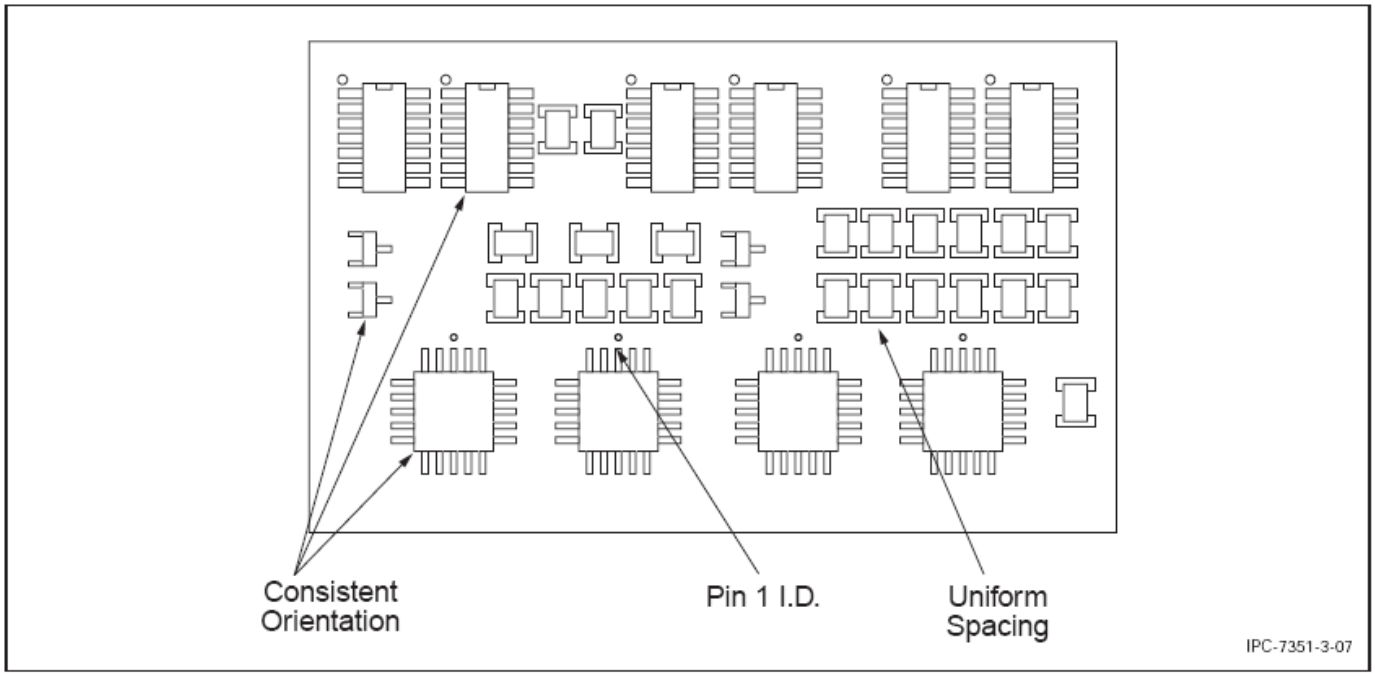


Figure 3-17 Alignment of Similar Components (Add some THTs!!)

3.4.2.1 Solder Paste Stencil The solder stencil is the primary vehicle by which solder paste is applied to the SMT PB. However, the stencil may also be used for intrusive soldering techniques where through-hole components are soldered into their respective holes during the reflow process.

Mixed SMT/Through-hole technology can use intrusive reflow soldering techniques. It is desirable to have a process where SMT and THT devices can be both:

a) Provided with printed solder paste
b) Placed or inserted into the PB
c) Reflowed together

The objective of stencil printing of solder paste for the intrusive reflow process is to provide enough solder volume after reflow to fill the hole and create acceptable solder fillets around the pins. Table 3-10 shows the process window for a typical solder intrusive soldering process.

Table 3-10 Process Window for Intrusive Soldering

	Maximum Limits	Desirable
Hole Diameter	0.65 - 1.60 mm	0.75 - 1.25 mm
Lead Diameter	Up to hole diameter minus 0.075 mm	Hole diameter minus 0.125 mm
Paste Overprinting	6.35 mm	< 4.0 mm
Stencil Thickness	0.125 - 0.635 mm	0.15 mm, 0.20 mm for fine-pitch

The optimum stencil thickness is determined by evaluating the solder paste requirements for all the components to be reflow soldered. This should be based on study of the minimum and target requirements for solder joints given in IPC/EIA-J-STD-001.

Ideally, the volume deposited should be the total amount required to achieve the ‘‘target’’ solder joint condition (see IPC-A-610), less the solder already available on the land and termination or lead (the latter can together amount to 10% to 20% of the total and should not be ignored). In making calculations, it should be noted that the solder content of most pastes is 50% to 55% by volume (not by weight), depending on particle size.

If the amount of solder paste to be deposited is less than the amount provided by using an aperture at or near the land area size, a reduced area of print should be placed in the best position on the land to assure good wetting of the joint areas. In some cases, this may best be achieved by reducing the width of the print, in others, the length. For very fine pitch with inter-land gaps of less than 0.2 mm, staggering (offsetting) the print at alternate ends of the lands can reduce the risk of shorts after soldering.

If the amount of solder paste required is more than the amount available using the geometry provided for the basic land pattern on the PB the aperture size in the stencil can be enlarged to increase solder volume. The amount and direction of the overhang of the printed solder beyond the land is dictated by the space available around the land and the need to avoid shorting and solder bridging if excess overhang occurs. The tolerances on land position and printing accuracy need to be

considered when calculating the maximum allowable over-print. See IPC-7525 for the design and fabrication of stencils for solder paste application.

3.4.3 Component Stand-off Height for Cleaning The recommended minimum component stand-off height for cleaning is affected by the distance across the diagonal of the component lead pitch. This is particularly important for large transformers or any through-hole part that might sit directly on the PB surface. The Dual-in-Line package was designed so that the leads guaranteed a space under the package for cleaning solution. See Table 3-11.

Table 3-11 Component Stand-off

Component Diagonal	Component Surface Area	Component Stand-off
≤ 50 mm	≤ 2500 mm^2	≥ 0.5 mm
≤ 25 mm	≤ 625 mm^2	≥ 0.3 mm
≤ 12 mm	≤ 144 mm^2	≥ 0.2 mm
≤ 6 mm	≤ 36 mm^2	≥ 0.1 mm
≤ 3 mm	≤ 9 mm^2	≥ 0.05 mm

If a minimum stand-off cannot be achieved, proper cleaning under the component may not be possible. In this case, it is recommended that a no-clean flux be used and/or mask material should be retained over all exposed via and circuit patterns located under devices.

3.4.4 Fiducial Marks A fiducial mark is a printed artwork feature created in the same process as the circuit artwork for optical recognition systems. The fiducial and a circuit pattern artwork must be etched in the same step.

The fiducial marks provide common datum points for all steps in the assembly process. This allows each piece of equipment used for assembly to accurately locate the circuit pattern. There are two types of fiducial marks.

3.4.4.1 Panel and Global Fiducials Global fiducial marks are used to locate the position of all circuit features on an individual PB. When a multi-image circuit is processed in panel form, the global fiducials are referred to as panel fiducials (see Figure 3-18).

A minimum of two global fiducial marks is required for correction of offsets (x and y position) and rotational offsets (theta position). These should be located diagonally opposite and as far apart as possible on the circuit or panel.

A minimum of three fiducial marks is required for correction of nonlinear distortions (scaling, stretch and twist). These should be located in a triangular position as far apart as possible on the circuit or panel.

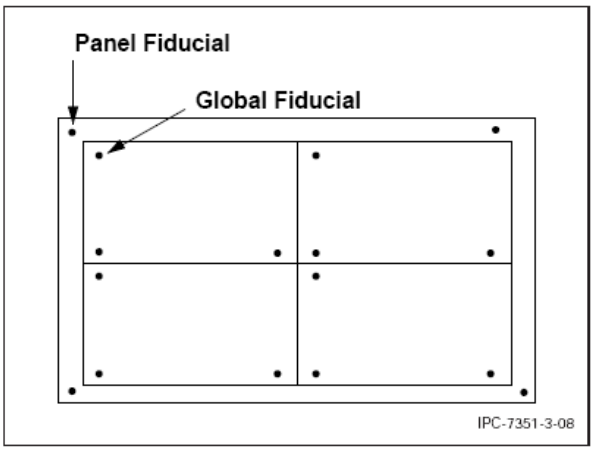


Figure 3-18 Panel/Local Fiducials

3.4.4.2 Local Fiducials Although local fiducial marks are usually used to locate the position of an individual component requiring more precise placement they are sometimes useful in providing an additional precision locator on a very large PB. In these instances the assembly pallet has the global fiducials which establish the outer periphery of the PB, while a set of local fiducials located near or at the center of the PB provide the additional precision check in order to machine insert large through hole components, such as the Pin Grid Array, especially if the hole to lead clearance is at a minimum.

A minimum of two local fiducial marks are required for correction of translational offsets (x and y position) and rotational offsets (theta position). This can be two marks located diagonally opposed within or outside the perimeter of the land pattern (see Figure 3-19).

It is good design practice to locate global or panel fiducials in a three-point grid-based datum system as shown in Figure 3-19. The first fiducial is located at the 0-0 location. The second and third fiducials are located in the X and Y directions from 0-0 in the positive quadrant. The global fiducials should be located on the top and bottom layers of all PBs that contain surface mount as well as through-hole components since even through-hole assembly systems are beginning to utilize vision alignment systems.

If two local fiducials are used to gain the extra precision it is useful to design the fiducial location into the component land pattern to insure that the location is available every time the component is placed, removed and/or replaced on the PB. In some instances the fiducials are placed randomly however their triangulation forms a centroid for the pallet location that can be used for the extra precision needed.

All fiducials should have a solder mask opening large enough to keep the optical target absolutely free of solder mask. If solder mask should get onto the optical target, some vision alignment systems may be compromised due to insufficient contrast at the target site.

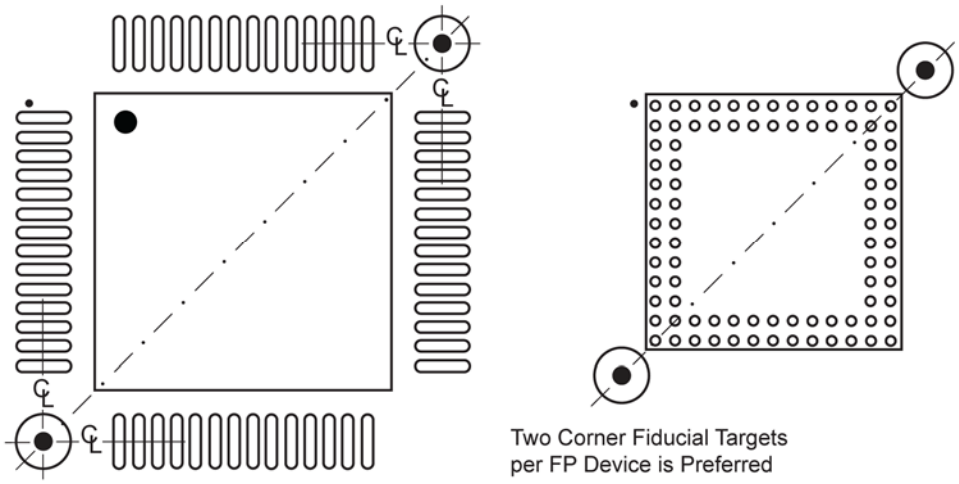


Figure 3-19 Local Fiducials

3.4.4.3 Size and Shape of Fiducial The optimum fiducial mark is a solid filled circle. The preferred diameter of the fiducial mark is 1.0 mm. The maximum diameter of the mark is 3.0 mm. Fiducial marks should not vary in size on the same PB more than 25 µm. A clear area devoid of any other circuit features or markings shall exist around the fiducial mark. The minimum size of the clear area shall be equal to twice the radius of the mark (see Figure 3-20).

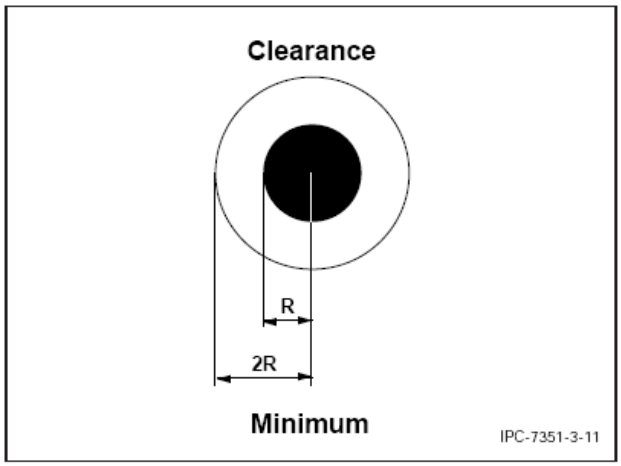


Figure 3-20 Fiducial Size and Clearance Requirements

3.4.4.4 Zonal Fiducials To ensure the accurate insertion of multiple leaded through-hole components that are not near ‘component specific local fiducials’ or ‘global fiducials’, additional ‘zonal fiducial targets’ may be placed within a zone or an area of the PB assembly to compensate for PB dimensional instability.

3.4.4.5 Material The fiducial mark may be bare copper, bare copper protected by organic coating or metal plating. If solder mask is used, it should not cover the fiducial mark or the clearance area. It should be noted that excessive oxidation of a fiducial mark’s surface may degrade its readability.

3.4.4.6 Flatness The flatness of the surface of the fiducial mark should be within 15 µm.

3.4.4.7 Edge Clearance The edge of the fiducial should be no closer to the PB edge than the sum of 4.75 mm and the minimum fiducial clearance required. If less than this sum, a PB handling fixture may be required.

3.4.4.8 Contrast Best performance is achieved when a consistent high contrast is present between the fiducial mark and the PB base material.

The background for all fiducial marks must be the same. That is, if solid copper planes are retained under fiducials in the layer below the surface layer, all fiducials must retain uniform background. If copper is clear under one fiducial, all must be clear.

3.4.5 Conductors

3.4.5.1 Conductor Width and Spacing Increased component density on many designs has mandated the use of thinner copper, narrower conductor width and spacing. Higher component density may increase PB layer counts as well, requiring the use of more vias to make the necessary connections between layers.

3.4.5.2 Inner Layer Conductors The use of wider conductors and spacing often drives layer counts up because there is less routing channel available between vias. It is for this reason that there is an increased usage of narrower conductors on internal layers. Since conductor width control is much more difficult to maintain on outer layers of the PB, it is better to keep the narrower conductor geometries on the inner layers of a multilayer PB. Generally, the option of using narrow geometries is driven by the need to reduce layer counts. Decreasing layer counts may reduce the overall PB thickness and improve the aspect ratio for small hole drilling.

3.4.6 Via Guidelines

3.4.6.1 Vias Under Components During wave soldering of the assembly, flux may potentially become trapped under zero clearance devices. If the assembly is to be wave soldered, via holes underneath zero clearance components on the primary side should be avoided on PBs unless vias are tented with solder mask. Non-tented via holes may be located underneath zero clearance surface mount packages in reflow soldered surface mount assemblies that will not be exposed to wave soldering (see Figure 3-21).

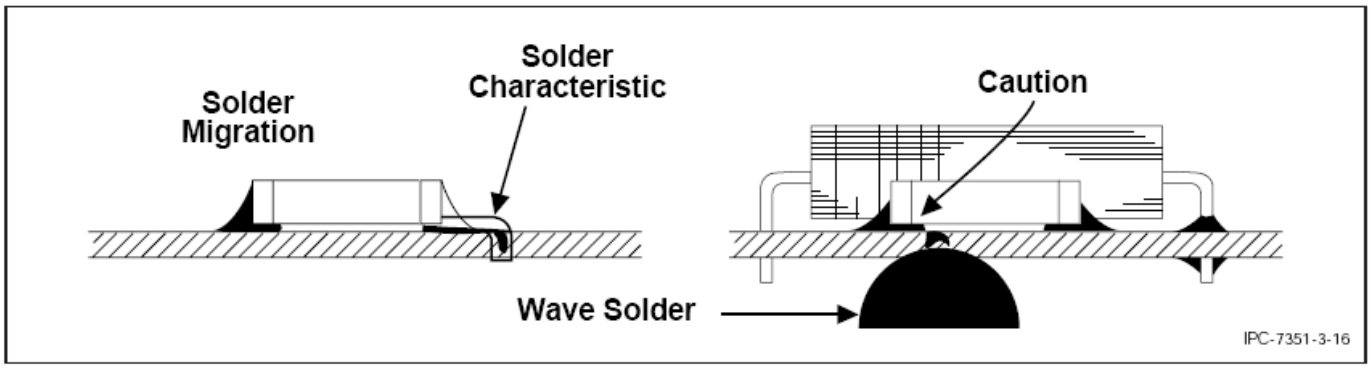
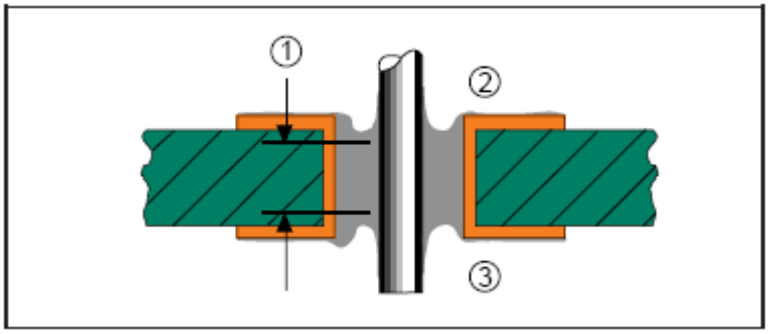


Figure 3-21 Vias Under Components

3.4.6.2 Vias as Test Points Via holes, in addition to being used for connecting surface mounted component lands to conductor layers, may also be used as test targets for bed-of-nails type probes and/or rework ports. When a via is used as a test point it is required that the x-y location and size of a test land be defined as a secondary file for test fixture development.

3.4.6.3 Component Hole Descriptions The requirements for component holes should consider automatic assembly of PBs with through-hole components, given specific consideration such that there is sufficient clearance between the hole and the lead for the insertion mechanism to perform its function. This standard considers the different levels of through-hole assembly and has maximized the lead to hole ratio in order to facilitate automatic insertion equipment, particularly for the Level A and B assembly processes. Since Level C contains requirements for higher component density applications, the lead to hole clearance may need to be evaluated based on the insertion equipment capability. Figure 3-22 shows the solder joint for a typical through-hole lead after insertion and wave soldering.



1. Vertical fill of solder meets requirements
2. Solder destination side
3. Solder Source Side

Figure 3-22 Through-hole Solder Joint

3.4.7 Standard PB Fabrication Allowances Manufacturing tolerances or standard fabrication allowances (SFA) exist in all PB fabrication shops. Virtually every registration or alignment operation that is performed has some potential for misregistration. There are approximately 42 basic steps in fabricating a multilayer PB, several of which involve operations that require precision in location and alignment. The tolerance varies according to the PB maximum diagonal dimension and must be included in the land size calculations. The fabricator should be consulted prior to beginning a design to determine their SFA. With this SFA value, the designer can proceed accordingly, preventing tolerances from stacking up and creating yield and/or production problems.

3.4.7.1 PB Manufacturing Characteristics Figure 3-22 shows the various characteristics of conductor geometry after etching. End-product drawings and specifications should specify only the minimum for conductor spacing; however, conductor widths should be defined according to minimum values, where land patterns should be defined as to their maximum material conditions (MMC). Clear target values for conductors and land patterns will help the manufacturer achieve the desired condition.

3.4.7.2 Conductor Width Tolerances Table 3-25 represents process tolerances that can be expected with normal processing. (Specific process tolerances should be discussed with the PB manufacturer.) The bilateral tolerances in Table 3-25 are typical for 0.046 mm [0.00181 in] copper. For additional copper thickness, a further width variation can be expected (see Figure 3-22).

3.4.7.3 Conductive Pattern Feature Location Tolerance Table 3-26 is for the tolerance to be applied to the nominal dimension chosen for the location of the lands, connector contacts and conductors in relation to the datum reference. These tolerances include master pattern accuracy, material movement, layer registration and fixturing.

3.4.7.4 Annular Ring Control Annular ring is defined as the amount of land that remains after a hole is drilled through it. With high-density SMT designs, maintaining minimum annular requirements has emerged as one of the most difficult parts of multilayer PB fabrication in terms of producibility. Perfect registration will maximize the annular ring all around the drilled hole.

For example, using a 0.8 mm [0.0315 in] land with a 0.5 mm [0.0197 in] drill will result in a 0.15 mm [0.00591 in] annular ring under perfect registration conditions. If misregistration of 0.15 mm [0.00591 in] occurs in any direction, the result will be a 0.3 mm [0.012 in] annular ring on one side of the pad, and no annular ring on the other side. If misregistration is greater than 0.15 mm [0.00591 in], i.e., 0.2 mm [0.0079 in], then the drill will actually break out of the land. If the breakout is in the direction where the conductor connects to the land, the drill will effectively disconnect the conductor from the land. The net result is a scrapped PB. Since signal conductors intersect the lands from all directions, any breakout has the potential to randomly disconnect conductors all over the PB.

Maintaining consistent annular ring control is difficult, but methods have been developed to insure connectivity between lands and conductors. Each method is intended to provide copper material where the conductor enters the land. The land which has the added material may resemble a teardrop or keyhole or adopt alternate designs as shown in Figure 3-23.

3.4.8 Panelization Components can be mounted on individual PBs or on PBs that are organized in a panel form. PBs or panels that will be moved by automatic handling equipment or pass through automated operations (parts placement, soldering, cleaning, etc.) must have specific areas kept free of parts or active circuitry. Typically, a clear area of 3.0 mm [0.012 in] to 5.0 mm [0.0197 in] wide must be allowed along the sides for the clearance. The required clearance width is dependent upon the design of the PB handling and fixturing equipment. These dimensions should be obtained from the process equipment manufacturer before PB or panel design (see Figure 3-24).

Special tooling and fixturing holes are generally located within the edge clearance areas. The clearance areas are needed to avoid interference with PB handling fixtures, guidance rails and alignment tools.

For accurate fixturing, two or more non-plated holes are located in the corners of the PB to provide accurate mechanical registration on PB transfer equipment. PB handling holes (typically 3.2 mm [0.126 in]) may also be located in the clearance areas. These holes may be used by automated PB handling equipment or for test fixture alignment. Specific panel size should be obtained from the equipment manufacturer or process engineer.

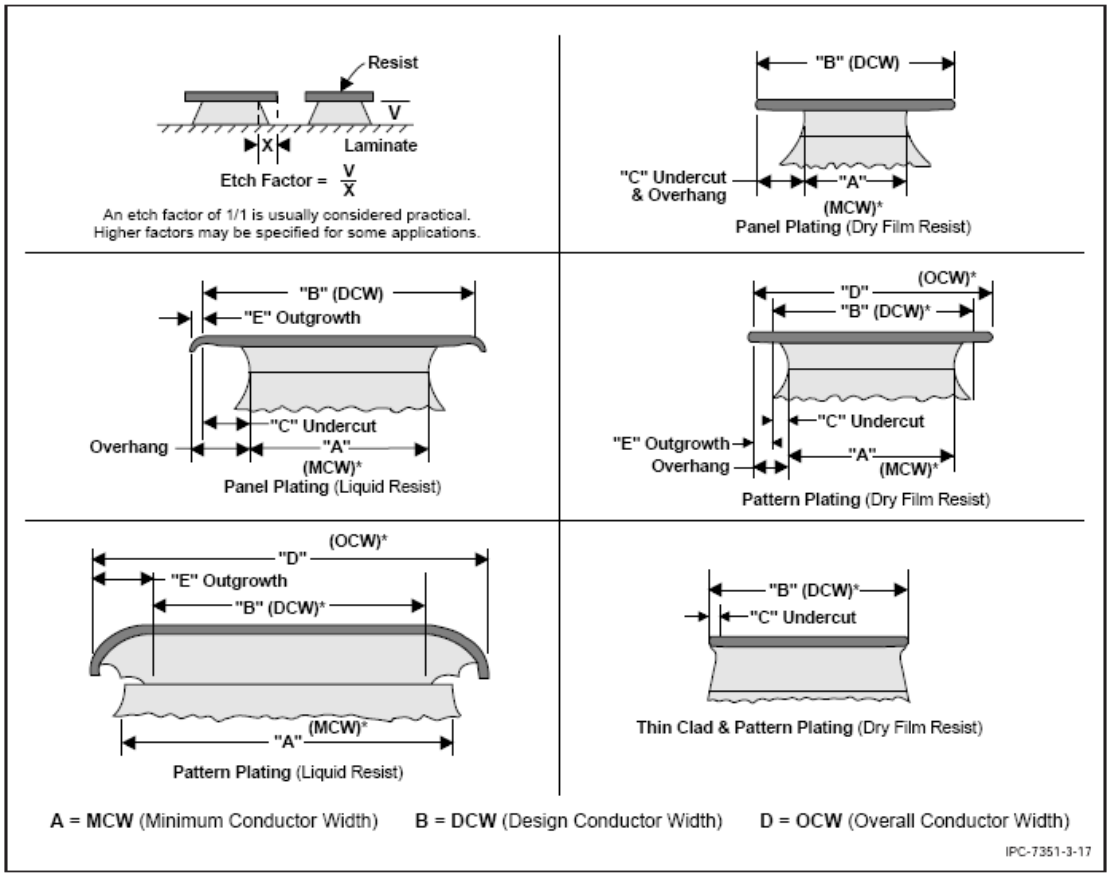


Figure 3-22 Conductor Description

Table 3-25 Conductor With Tolerances, 0.046 mm [0.0018 in] Copper, mm [in]

Feature	Producibility Level A	Producibility Level B	Producibility Level C
Without plating	± 0.06 mm [± 0.00236 in]	± 0.04 mm [± 0.00157 in]	± 0.015 mm [± 0.0005906 in]
With plating	± 0.10 mm [± 0.00393 in]	± 0.08 mm [± 0.00314 in]	± 0.05 mm [± 0.0197 in]

Table 3-26 Feature Location Accuracy (units: mm [in])

Greatest PB/ X,Y Dimension	Producibility Level A	Producibility Level B	Producibility Level C
Up to 300 [11.81]	0.30 [0.012]	0.20 [0.00787]	0.10 [0.00394]
Up to 450 [17.72]	0.35 [0.0138]	0.25 [0.00984]	0.15 [0.00591]
Up to 600 [23.62]	0.40 [0.0157]	0.30 [0.012]	0.20 [0.00787]

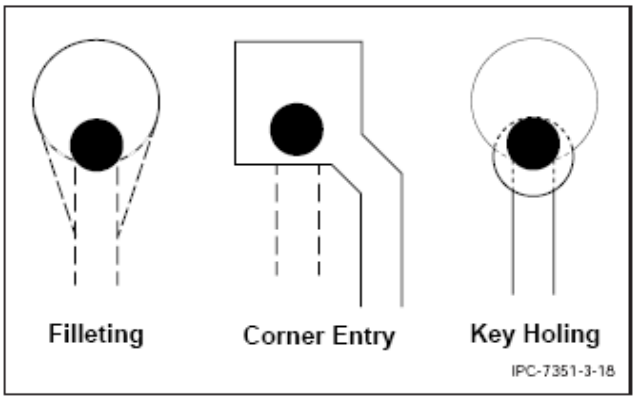


Figure 3-23 Examples of Modified Landscapes

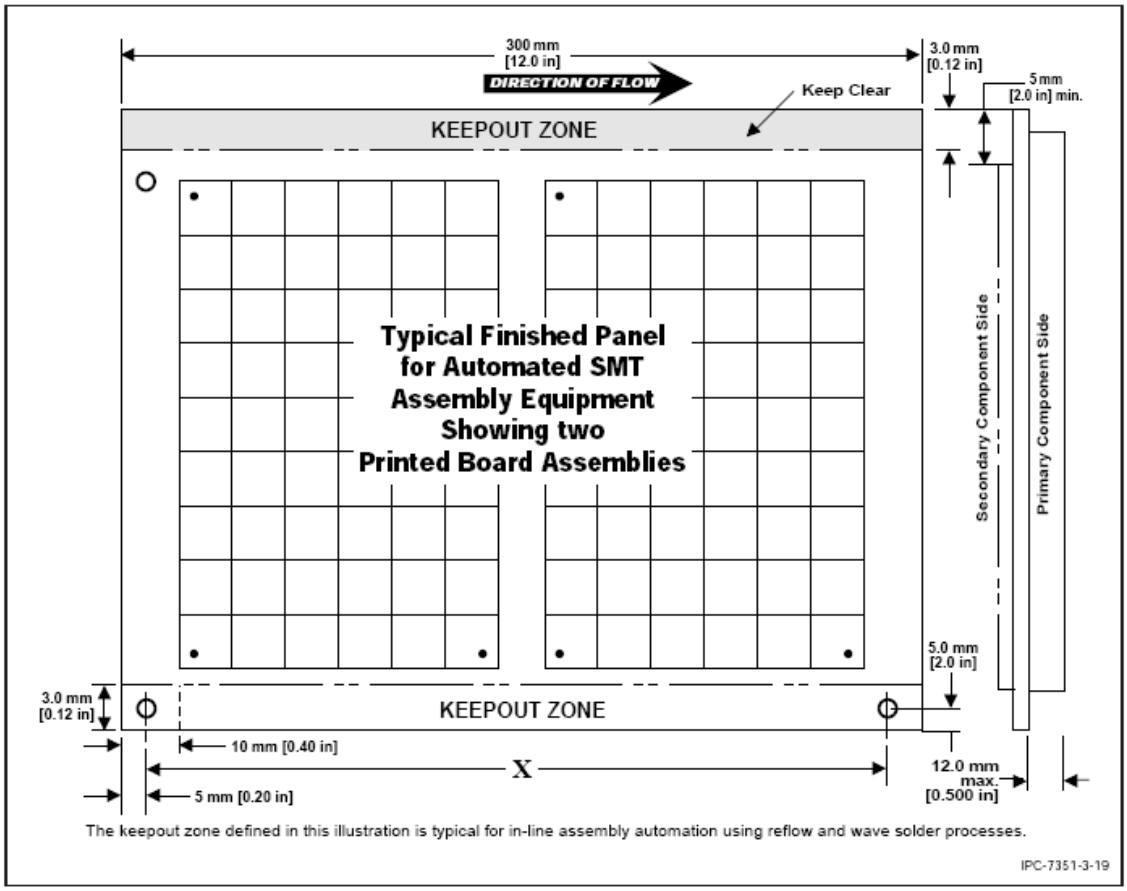


Figure 3-24 Typical Copper Glass Laminate Panel

3.4.8.1 PB Size and Panel Construction In order to fully utilize the automation technology associated with high density components, a designer should consider how a PB or P&I structure will be fabricated, assembled and tested. Each of these processes, because of the particular equipment used, may require fixturing, which will affect or dictate certain facets of the PB layout. Tooling holes, panel size, component orientation and clearance areas (both component and conductor) on the primary and secondary sides of the PB are all equipment and process dependent.

To produce a cost-effective layout through optimum base material utilization, a designer should consult with the PB manufacturer to determine optimum panel size. The PB should be designed to utilize the manufacturer's suggested usable area. Smaller PBs can be ganged or nested in a uniform panel format to simplify fixturing and reduce excessive handling during assembly. Panel layout is typically defined by an assembly process specialist or the manufacturing service provider.

Panel construction may include several PBs arranged in a matrix or simply one PB requiring additional material retained for efficient assembly processing. The large PB or several smaller PBs are retained in the panels and separated after all assembly processes are completed. Excising or separating the individual PBs from the panel must be planned as well. Several methods are used to retain circuits in a panel, including V-groove scoring, NC routing and routed slot with break-away tabs.

3.4.8.2 V-Groove Scoring V-groove scoring may be provided to enable post assembly separation. The groove feature is generally provided on both surfaces of the PB and only in a straight line. A small cross-section of PB material is retained at

the break line. An allowance for the scoring angle must be made as well. Conductors that are located too close to the score groove will be exposed or damaged, and rough edges must be sanded lightly to remove burrs and rough fabric particles (see Figure 3-25).

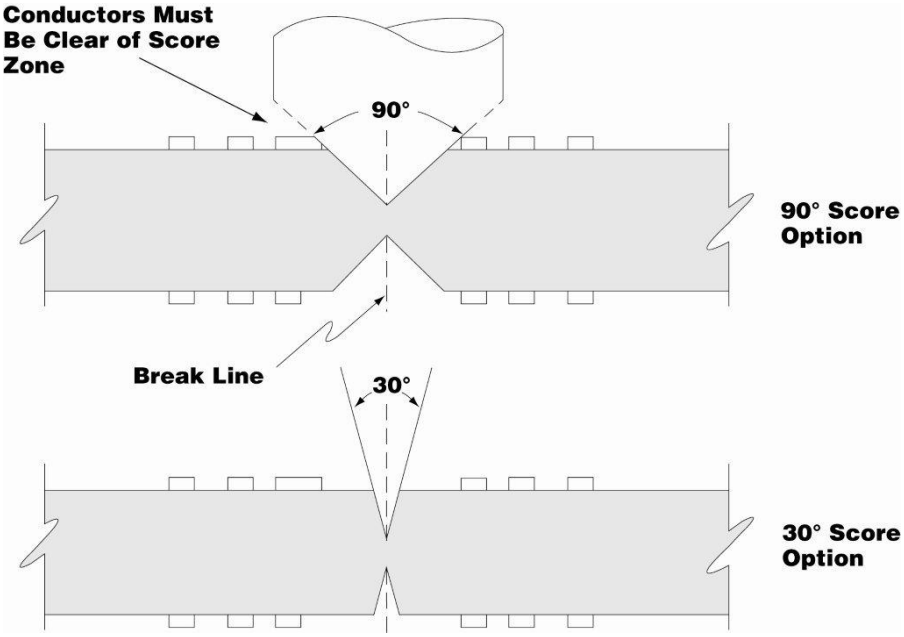


Figure 3-25 Conductor Clearance for V-Groove Scoring

3.4.8.3 Routed Slot and Tab Features The routed slot and tab pattern is widely used for panel construction and break-away tab extensions. Routing is more precise than scoring, and edge surfaces are smooth, but the break-away ‘‘tab’’ points will require consideration. Tabs can be cut and ground flush with the PB edge or predrilled in a pattern. The drilled pattern furnishes a low stress break point on the ‘‘tab.’’ If the hole pattern is recessed within the PB edge, secondary sanding or grinding can be bypassed (see Figure 3-26).

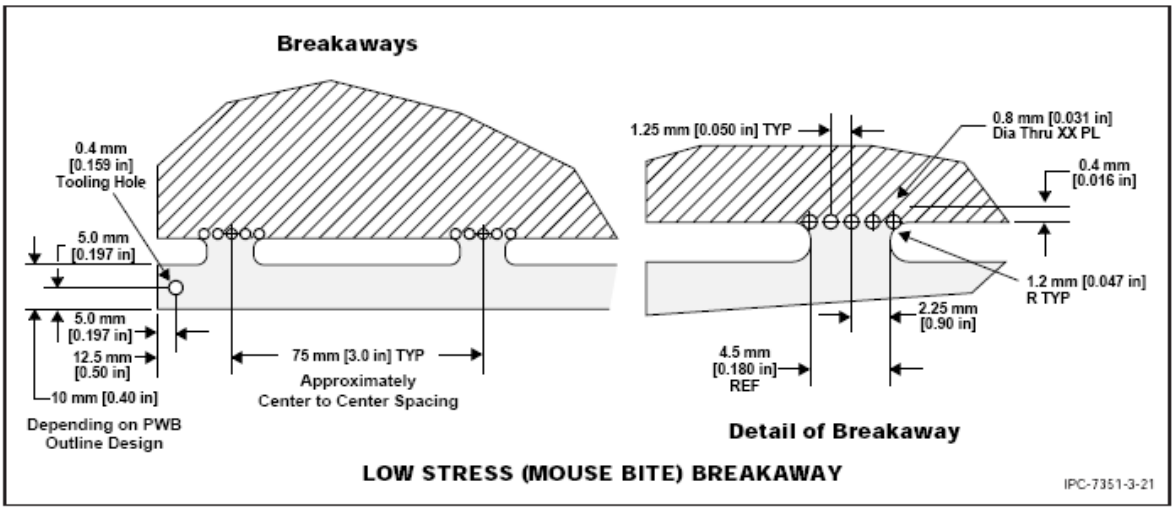


Figure 3-26 Breakaway (Routed Pattern) with Routed Slots

3.5 Outer Layer Surface Finishes

3.5.1 Solder Mask Finishes Solder mask coatings are used to protect the circuitry on the PB. Solder mask coatings are available in two forms, liquid and dry film. The polymer mask material is applied using several process methods and is furnished in varying thicknesses. As an example, liquid materials will have a finished thickness of 0.02 mm [0.0079 in] to 0.025 mm [0.00984 in] while the dry film products are supplied in thicknesses of 0.04 mm [0.016 in], 0.08 mm [0.0315 in], and 0.10 mm [0.0394 in]. Although screen type printing for solder mask is available, photo-imaged solder mask is recommended for surface mount applications.

The photo process provides a precise pattern image and when properly developed eliminates mask residue from land pattern surfaces. The mask thickness may not be a factor on most surface mount assemblies but, when fine pitch (0.63 mm [0.0248 in] or less) IC devices are mounted on the PBs, the lower profile solder mask will provide better solder printing control.

3.5.3 Land Pattern Surface Finishes The solder mask openings expose the land patterns for attachment of through-hole and surface mount components. These are usually copper-based and therefore need protection in order to prevent the copper from oxidizing, thus resulting in poor solderability of the surface land patterns. The protection of the land patterns may be accomplished by organic solderability protective (OSP) coatings or metallic finishes such as solder coating, gold, silver, or palladium plating.

The choice of coatings or plating is dependent on the assembler's preference or the type of components being assembled. A single coating or plating finish is preferred for the entire PB. Mixing the surface finish types is not recommended due to the different process steps required. Selective finishes may be necessary based on the mix of component types, lead pitch and attachment process or lead termination finish characteristics.

The surface finish of the PB may need to perform any of the following functions: solderability protection, conductive surface for contacts/switches, wire bonding surface, and solder joint interface. A variety of components and assembly operations of the PB must be taken into consideration when choosing the most appropriate surface finish. There is no single surface finish that will be ''best'' for all applications. Some of the most commonly used surface finishes are: hot air solder leveling (HASL), organic surface protection (OSP), immersion tin, and noble coatings (including electroless nickel/immersion gold, electrolytic nickel/electroplated gold and immersion/silver).

Some of the application features that must be considered in selection of a suitable surface finish are given in Table 3-27. Although most HASL alloys consisted of Tin/Lead composition, with the advent of moving to lead free solders, the new HASL processes consist of a combination of Tin/Copper to accomplish the surface finish. Ironically, because of the new alloy flow characteristics, the HASL lands appear to be much flatter than the original Tin/Lead alloy versions. The caution, however, is that PB material and plated through hole structure must withstand a slightly higher temperature.

Table 3-27 Key Attributes for Various PB Surface Finishes

	HASL SnPb/SnCu*	OSP	Electroless Ni/ Immersion AU	Electrolytic Ni/ Electroplated AU	Immersion Silver**	Immersion Tin
Shelf Life proper Handling	1 Year	6 Months	>1 Year	>1 Year	6 Months	6 Months
Handling	Normal	Avoid physical contact	Normal	Normal	Avoid physical contact	Avoid physical contact
SMT land Surface topology	Domed/Flatter	Flat	Flat	Flat	Flat	Flat
Multiple assembly reflow cycles	Good, although intermetallics increase/need robust laminate	Fair, better with thick coatings; may see bare copper if reflowed with lead-free solder paste	Good	Good	Good	Good
Soldering Fluxes and Atmospheres	No Concerns	May require more aggressive fluxes/and Nitrogen Atmosphere	No concerns	No concerns	Possible flux residue incompatibility	Possible flux residue incompatibility
Use on thick PCBs	Barrels difficult to fill and clear	PTH fill concerns	Improved barrel reliability	Improved barrel reliability	PTH fill concern	PTH fill concern
Use in thin PCBs	No, prone to warping/Avoid	Yes	Yes	Yes	Yes	Yes
Solder joint reliability	Good	Good	BGA "black pad" concerns	Gold embrittlement concerns	Planar microvoid concerns	Good
			Sporadic brittle fracture			
Card edge contacts	Additional plating operation	Additional plating operation	Additional plating operation	No additional plating	Additional plating operation	Additional plating operation
Wire bonding	No	No	No	Yes	Yes	Yes
Test point probing	Good	Poor, unless solder applied during assembly	Good	Good	Good	Good
Exposed Copper after Assembly	No	Yes	No	No	No	No
Switches/Contacts	No	No	Yes	Yes	Yes	No
Waste Treatment and Safety in PCB Fabrication	Poor/Fair	Good	Fair	Fair	Poor	Good
Process Control	Thickness control concerns	Fair	Phosphorus content concerns	Gold thickness control concerns	Microetch and plating concerns	Tin whisker concerns
Coating thickness/µm	0.8 - 0.38	0.2 - 0.5	3-7/0.05 - 0.10	0.8 - 2.5	0.07 - 0.10	1.0 - 1.3
General Cost Comparison	1	0.4 - 0.6	2.0 - 3.0	1.2 - 1.5	1.1 - 1.6	~0.8

* Tin copper alloy is the preferred alloy for lead-free HASL
** For reflow operation >1 year if sealed in Moisture Membrane Bag (MMB)

4 COMPONENT QUALITY VALIDATION

4.1 Validation Techniques Because of the variety of component tolerances, and the possibility that tolerances may vary on components, users are encouraged to establish validation of the land pattern and component geometry. In addition, components should be selected and qualified to meet the end products maximum operating temperature limits. Figure 4-1 shows a chart referencing the upper and lower limits of various components.

Validations of parts and circuits may be accomplished through the use of standard test patterns. These patterns may be used not only to evaluate a particular part to a land pattern, but may also be used to evaluate component products' capability to stand up to various processes being used in assembling surface mounted parts.

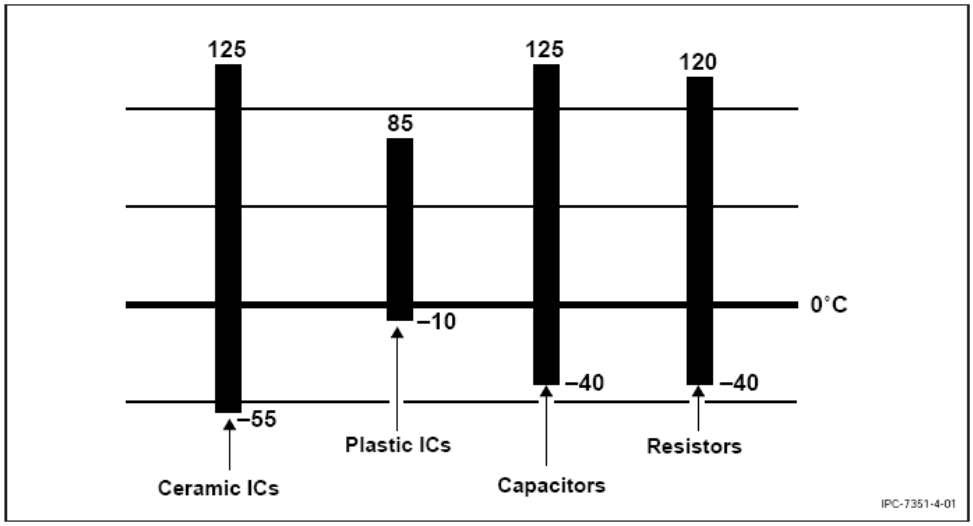


Figure 4-1 Component Operating Temperature Limits

5 TESTABILITY

5.1 PB and Assembly Test There are five basic types of tests which can be performed on PBs. These are:

a) Bare-PB test which checks the unpopulated PB for shorts and opens
b) Manufacturing defect analysis which checks the populated PB for soldering shorts
c) In-circuit test operational verification of each individual component
d) Functional test operational verification of functional block of circuits
e) Combinational test limited integration of in-circuit and functional test

The first test type is a bare-PB test performed by the PB fabricator. The remaining four test types are loaded on assembled PB tests and performed after assembly. The bare-PB test should be mandatory, while the loaded PB may be tested using any one or a combination of the four loaded PB tests.

5.1.1 Bare-PB Test In testing PBs using through-hole technology, the defect rate and the test methods chosen are the principal determiners of overall test cost. Real-estate considerations (specifically the percentage of nodes that are available for bed-of-nails probing) are not a concern, since the holes provide 100% nodal access. In testing surface mount PBs, however, real-estate considerations (in addition to defect rates) have an impact on test costs, since nodal access determines which test methods are possible and effective.

The use of design concepts with grid-based 100% nodal access from either side of the PB may be the most economical approach from the total process perspective. If the grid-based test land concept is used, the test fixtures for bare and assembled PB tests will not become obsolete through later PB connectivity revisions if the test nodes are not moved. Also, if the PB uses buried vias, the grid-based test land concept with 100% nodal access may provide access to buried nets from the ends of the nets; this is a benefit realized during the bare-PB test.

5.1.2 Assembled PB Test The method of test must be determined prior to design layout. If the defect rate is relatively high, most PBs will require diagnosis, and the economics of automatic in-circuit test (ICT) will demand that full nodal access be provided within the PB layout. If the defect rate is low, ICT may be omitted and rely on a functional test. Extremely low defect levels would theoretically allow 0 % nodal access (no bed-of-nails test at all), applying only a simple pass/no-pass test through a common interface connector.

The major considerations in determining nodal access are:

- Defect rate
- Diagnostic capability
- Real-estate impact
- PB area
- Layer count
- Cost impact

Determining the percentage of nodal access to design into a PB layout requires trading off all the issues discussed previously: defect rate, test development cost, test operation costs including manual troubleshooting costs, and, of course, impacts on real estate. Short of having no defects at all, full nodal access remains the most desirable option.

With through-hole technology PBs, once the PB is designed (nodal access fixed) and its tests are designed (test methods fixed), the defect rate becomes the primary key to reducing test costs. Therefore, defect reporting, analysis, and correction/prevention are imperative. This may involve closer supplier relationships to reduce component and PB level problems, and in-house action to reduce process-induced problems.

5.2 Nodal Access In the early stages of product development cycles, test philosophies and strategies are often undefined. This is especially true when a company is moving from one level of packaging technology to the next higher level of packaging technology; for example, from through-hole technology to surface mount technology or from fine-pitch lead-frame packaged ICs to BGA or CSP. During these transition periods, the concurrent engineering approach is essential for designing nodal access for testability into the product. Concurrent engineering is the principal vehicle by which test priorities can and should be moved up to the beginning of the design cycle and addressed with a higher priority. In the early stages of a design, a test philosophy should be clearly defined, then a strategy for executing the tests can be implemented. An ideal philosophy to adopt is one that identifies all of the different test types and the level of test that each type requires.

5.2.1 Test Philosophy The test philosophy should be written to encompass whatever combination of tests are necessary for the product. Then, a simple strategy for implementing the required tests can be defined prior to beginning the design process. Planning testability at the beginning of a product development cycle instead of the end can result in significantly lower test costs per node and provide higher nodal accessibility throughout the entire process from initial design to final test.

The best test philosophy to adopt is one that will make provisions for executing every test method available. Even when the product testing procedure is well defined at the beginning of the development cycle, it may change after the design is complete. Some things to consider in outlining a test philosophy:

a) Strategic placement of all surface mount component vias

b) Strategic fanout of through-hole component test probing sites

c) Provide access to every node of every net

d) Access of every node from one side of the PB is preferred

e) Correct test land or via geometries and clearances.

Even in the higher density designs, the philosophy of providing 100% access to every node of every net from either side of the PB can be accomplished. However, this decision must be made at the beginning of a design.

5.2.2 Test Strategy for Bare PBs After the product test philosophy has been established, a test strategy or procedure can be defined. For an overview of several elements of a procedure, consider the following:

a) Vision inspection of inner layers using AOI

b) Vision inspection of O/L land/via connections

c) Probe only vias on either side for bare PB test

d) Do not damage test location lands with probe tips

e) Probe secondary side vias for loaded test PB

f) Screen paste on vias for airtight PB or fill vias with resin

The actual product test strategy must be organized by all of the concurrent engineering team members who will be involved in the testing process. This will ensure that the integration of the various test types and procedures will not have too much redundancy, or create gaps that may endanger test integrity.

5.3 Full Nodal Access for Assembled PB The number of test probes needed to test the PB is equal to the total number of device nodes or common connection between devices. However, in the case of the most dense application designs, this often requires the use of a double-sided, or clamshell test fixture because all of the nodes are not accessible from one side of the PB.

In-Circuit Test (ICT) only needs to have access to one node per net. Every net has at least two nodes. Some nets have many nodes, for example, on memory PBs one net may be connected to many nodes. In order to achieve full integrity at the ICT level, access to only one node of each net is all that is required. Therefore, the total number of test probes required to perform the ICT is significantly less than the number required for the bare PB test.

For large pin-out through-hole device components, it is good design practice to distribute the test vias fanned out, or in, as the component design will allow in order to minimize the stress placed on the PB from the probe pins during ICT as shown in Figure 5-1. This accomplishes two objectives:

a) The maximum density of test points established for a given piece of test equipment is not exceeded.

b) Wider distribution of test points reduces the high-pressure point areas which cause fixture bowing during vacuum or mechanical actuation.

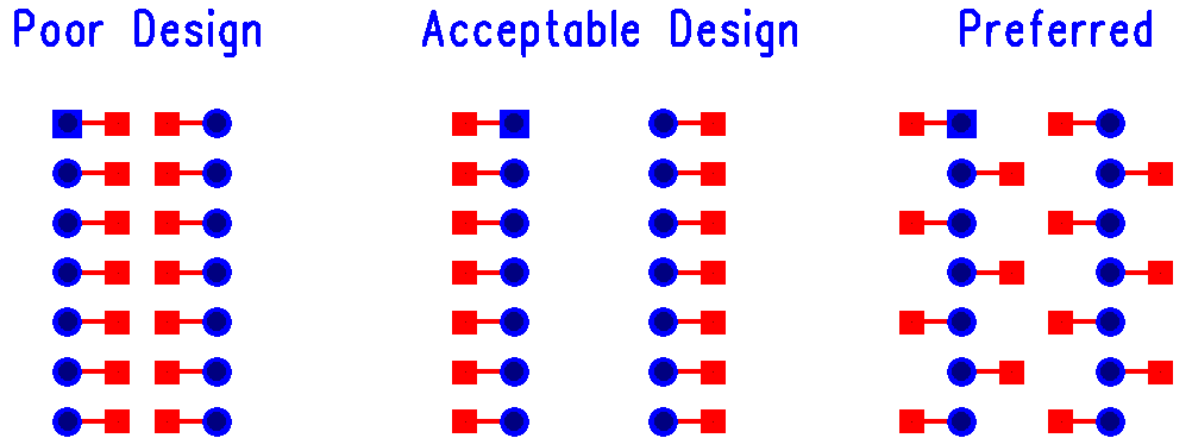


Figure 5-1 Test Via Grid Concepts (Features a 1.0 mm Probe Land Edge to Component Mounting Land Edge Clearance)

5.3.1 In-Circuit Test Accommodation Specific via lands and holes can be reserved and accessed for automatic ICT. The via land location for each common network in a circuit is matched to a test probe contact in the test fixture. The test system can then drive each device on the assembly and quickly locate defective devices or identify assembly process problems.

To insure precise alignment of the probe contact pins with the PB, exact x and y probe position and specific networks must be furnished to the fixture developer. Identifying the test locations as components in the CAD database will allow for easy transfer of fixture drilling data. This data will reduce fixture development time and eliminate the drilling of excessive, nonfunctional holes in the fixture base. For low volume assembly, or high component density assembly, fixtureless testing by way of flying probe equipment is an option.

5.3.2 Multi-Probe Testing Some test probe systems can exert considerable deformation forces on the assembled PBs and are a known source of premature service failures. An essential part of the PB layout is to ensure that the location of probing points on the PB are staggered at sufficient distances to avoid excessive deformation during multi-probe testing. When the probe point locations are highly concentrated, additional support may be needed in the test fixture design in order to counter the effect against the high probe pressure concentration. The area on the PB where the support is to be provided should be located where it is clear of conductors and components.

5.4 Limited Nodal Access Provided the designer has allowed sufficient room for access to the test land(s), limited nodal access (less than 100%) still allows the use of spring probe (bed-of-nails) testing, but not as effectively as full nodal access does. When nodal access is less than 100%, shorts, defects and in-circuit testing cannot be performed completely, and some faults may not be detected.

A greater burden is therefore placed on functional or system test to detect and diagnose shorts, defects, and bad devices. This burden varies inversely with the nodal access percentage. The extra effort at functional test may consist of additional recurring manpower cost to diagnose failing PBs, or it may mean developing a more detailed functional test (nonrecurring cost) than would have been planned otherwise.

5.5 No Nodal Access No nodal access (0%) prohibits bed-of-nails testing and defers all assembly defects and component testing until the functional or system test bed. This can only be cost-justified if the much higher cost-per defect repair is performed so infrequently that the total cost is less than the cost of developing and operating an ATE bed-of-nails test. In other words, the first pass yields must be extremely high to justify this approach.

5.6 Clam-Shell Fixtures Impact Probing the PB from both sides requires a ‘‘clam-shell’’ type of fixture. These are expensive, take more time to fabricate, require larger test lands on the primary side to protect against registration problems due to tolerance stack-ups, and they are more difficult to maintain.

5.7 PB Test Characteristics

5.7.1 Test Land Pattern Spacing Design for testability is as much a part of the schematic design process as it is a part of the PB layout process. Ideally, the PB would have 100% of the nodes accessible from the secondary side of the PB assembly. In-circuit testers must have access to at least one node per net. Probe spacing is optional; however, standard probe spacing is typically 2.0 mm [0.0787 in] to 2.5 mm [0.0984 in] while miniature, needle type probes can be spaced as close as 1.0 mm [0.0394 in] to 1.25 mm [0.04921 in].

The drawbacks to the 1.0 mm [0.0394 in] to 1.25 mm [0.04921 in] grid-based test lands are the following. The miniature, needle type probes are more expensive and they do not hold up as well in high-volume production. Also, any via sites that are to be used as test points should be solder filled for better contact and increased probe life.

5.7.2 Test Land Size and Shape Lands or vias should be 0.9 mm [0.0354 in] to 1.0 mm [0.0394 in] for probing. As land sizes decrease, misses increase dramatically as shown in Figure 5-2. The use of square via lands may provide a larger target zone for the test probe to contact.

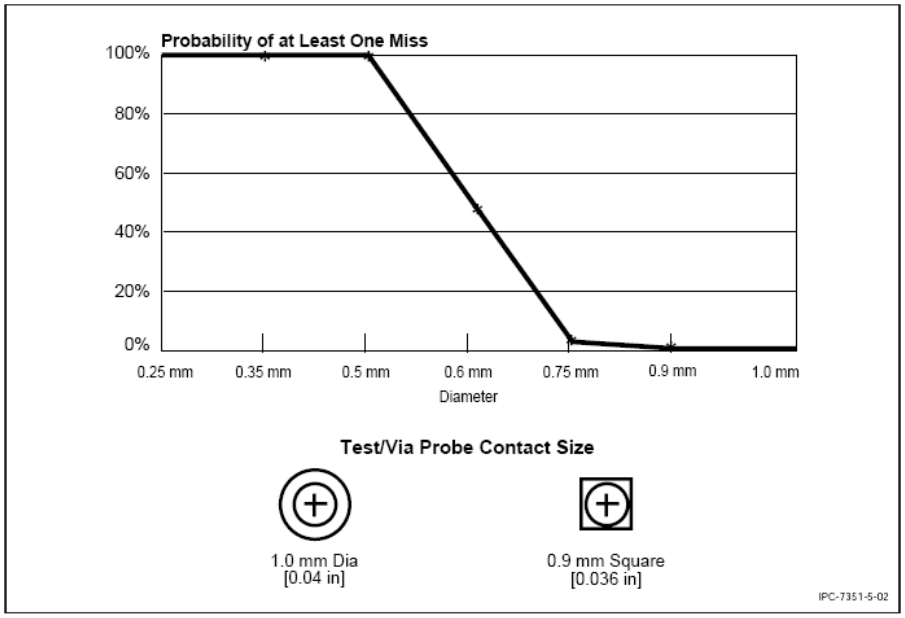


Figure 5-2 General Relationship between Test Contact Size and Test Probe Misses

5.7.3 Design for Test Parameters The following other considerations are important to the general land pattern design that should be incorporated into the PB:

a) Two non-plated tooling holes should be available on opposite corners of the PB

b) Test lands should be 2.5 mm [0.0984 in] minimum from the edge of the PB to facilitate gasketing on vacuum fixtures

c) When using vias for test points, caution should be taken to insure that signal quality is not degraded at the expense of testing capability

d) Test lands should be 0.63 mm [0.0248 in] minimum from mounting land areas

e) Where possible, provide numerous test lands for power and ground

f) Where possible, provide test lands for all unused gates. Free running gates sometimes cause instability during in-circuit testing. This will provide a means of grounding these spurious signals

It is sometimes desirable to provide drive and sense nodes test lands to perform six-wire bridge measurements during in-circuit test. Directions for this should come from test engineering.

In addition, it is useful to identify the test vias and lands on an assembly drawing in event of the need to modify the circuit topology. Changes made without moving test lands avoid fixture modification, saving cost and time.

Care should be taken when mounting components on the secondary side to avoid covering a via hole that is a designated test land. Also, if a via hole is too close to any component, damage may result to the component or fixture during probing (see Figure 5-3).

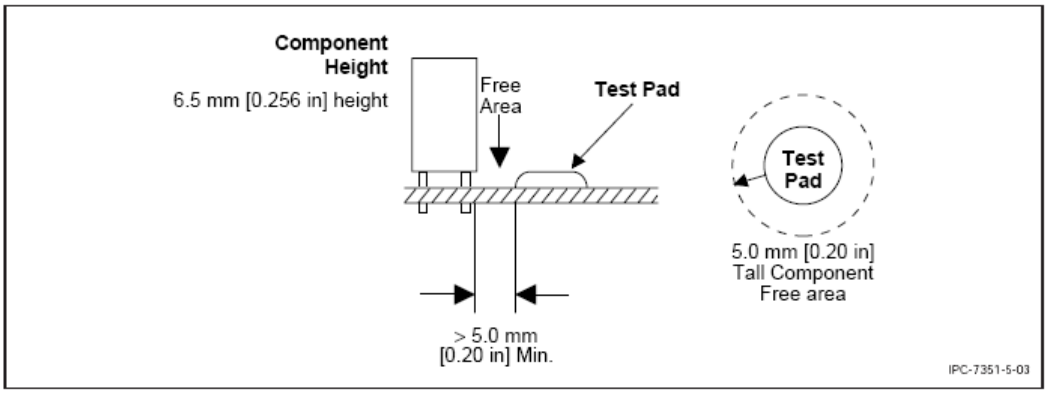


Figure 5-3 Test Probe Feature Distance from Component
(To be Updated by Tom Hausherr)

6 PB STRUCTURE TYPES

The selection of a packaging and interconnecting structure for through-hole mounting applications is important for optimum thermal, mechanical and electrical systems reliability. Each candidate structure has a set of properties with particular advantages and disadvantages when compared to others (see Table 6-1).

It is probable that no one packaging and interconnecting structure or PB will satisfy all of the needs of the application. Therefore, a compromise of properties should be sought that offers the best ‘‘tailoring’’ for component attachment and circuit reliability.

Table 6-1 PB Structure Comparison

Type	Major Advantages	Major Disadvantages	Comments
Organic Base Substrate Epoxy fiberglass	Substrate size, weight, rework-able, dielectric properties, conventional PB processing.	Thermal conductivity, X, Y and Z axis CTE.	Because of its high X-Y plane CTE, it should be limited to environments and applications with small changes in temperatures and/or small packages.
Polyimide fiberglass	Same as epoxy fiberglass plus high temperatures X-Y axis CTE, substrate size, weight, reworkable, dielectric properties, high Tg.	Thermal conductivity, Z-axis CTE, moisture absorption.	Same as epoxy fiberglass.
Epoxy aramid fiber	Same as epoxy fiberglass, X-axis CTE, substrate size, lightest weight, reworkable, dielectric properties.	Thermal conductivity, Z-axis CTE, resin microcracking, Z axis CTE, water absorption.	Volume fraction of fiber can be controlled to tailor X-Y CTE. Resin selection critical to reducing resin micro-cracks.
Polyimide aramid fiber	Same as epoxy aramid fiber, X-axis CTE, substrate size, weight, reworkable, dielectric properties.	Thermal conductivity, Z-axis CTE, resin microcracking, water absorption.	Same as epoxy aramid fiber.
Polyimide quartz (fused silica)	Same as polyimide aramid fiber, X-Y axis CTE, substrate size, weight, reworkable, dielectric properties.	Thermal conductivity, Z-axis CTE, drilling, availability, cost, low resin content required.	Volume fraction of fiber can be controlled to tailor X-Y CTE, drill wear-out higher than with fiberglass.
Fiberglass/aramid composite fiber	Same as polyimide aramid fiber, no surface microcracks, Z axis CTE, substrate size, weight, reworkable, dielectric properties.	Thermal conductivity, X and Y axis CTE, water absorption, process solution entrapment.	Resin microcracks are confined to internal layers and cannot damage external circuitry.
Fiberglass/PTFE® laminates	Dielectric constant, high temperature.	Same as epoxy fiberglass, low-temperature stability, thermal conductivity, X and Y axis CTE.	Suitable for high-speed logic applications. Same as epoxy fiberglass.

Flexible dielectric	Light weight, minimal concern to CTE, configuration flexibility.	Size, cost, Z-axis expansion.	Rigid-flexible PBs offer trade-off compromises.
Thermoplastic	3-D configurations, low high-volume cost.	High injection-moulding setup costs.	Relatively new for these applications.
Nonorganic Base Alumina (ceramic)	CTE, thermal conductivity, conventional thick film or thin film processing, integrated resistors.	Substrate size, rework limitations, weight, cost, brittle, dielectric constant.	Most widely used for hybrid circuit technology.
Supporting Plane PB bonded to plane support (metal or nonmetal)	Substrate size, reworkability, dielectric properties, conventional PB processing, X-Y axis CTE, stiffness, shielding, cooling.	Weight.	The thickness/CTE of the metal core can be varied along with the PB thickness, to tailor the overall CTE of the composite.
Sequential processed PB with supporting plane core	Same as PB bonded to supporting plane.	Weight.	Same as PB bonded to supporting plane
Discrete wire	High-speed interconnections, good thermal and electrical features.	Licensed process, requires special equipment.	Same as PB bonded to low-expansion metal support plane.
Constraining Core Porcelainized copper-clad invar	Same as alumina.	Reworkability, compatible thick film materials.	Thick film materials are still under development.
PB bonded with constraining metal core	Same as PB bonded to low expansion metal cores, stiffness, thermal conductivity, low weight.	Cost, microcracking.	The thickness of the graphite and PB can be varied to tailor the overall CTE of the composite.
Compliant layer structures	Substrate size, dielectric properties, X-Y axis, CTE.	Z-axis CTE, thermal conductivity.	Compliant layer absorbs difference in CTE between ceramic package and substrate.

6.1 General Considerations PB structures vary from basic PBs to very sophisticated supporting-core structures. However, some selection criteria are common to all structures. To aid in the selection process, Table 6-2 lists design parameters and material properties which affect system performance, regardless of PB type. Also, Table 6-3 lists the properties of the materials most common for these applications.

Table 6-2 PB Structure Selection Considerations

Design Parameters	**Material Properties**								
	Transition Temperatures	**Coefficient of Thermal Expansion**	**Thermal Conductivity**	**Tensile Modulus**	**Flexural Modulus**	**Dielectric Constant**	**Volume Resistivity**	**Surface Resistivity**	**Moisture Absorption**
Temperatures and power cycling	X	X	X	X					
Vibration				X	X				
Mechanical shock				X	X				
Temperatures and humidity	X	X				X	X	X	X
Power density	X		X						
Chip carrier size		X		X					
Circuit density						X	X	X	
Circuit speed						X	X	X	

Table 6-3 PB Structure Material Properties

Material	Material Properties							
	Glass Transition Temperature	**XY Coefficient of Thermal Expansion**	**Thermal Conductivity**	**XY Tensile Modulus**	**Dielectric Constant**	**Volume Resistivity**	**Surface Resistivity**	**Moisture Absorption**
Unit of Measure	°C	PPM/°C (Note 4)	W/M°C	PSI x 10^{-6}	At 1 MHz	Ohms/cm	Ohms	Percent
Epoxy fiberglass	125	13-18	0.16	2.5	4.8	10^{12}	10^{13}	0.10
Polyimide fiberglass	250	12-16	0.35	2.8	4.8	10^{14}	10^{13}	0.35
Epoxy aramid fiber	125	6-8	0.12	4.4	3.9	10^{18}	10^{16}	0.85
Polyimide aramid fiber	250	3-7	0.15	4.0	3.6	10^{12}	10^{12}	1.50
Polyimide quartz	250	6-8	0.30		4.0	10^{9}	10^{8}	0.50
Fiberglass/ Teflon®	75	20	0.26	0.2	2.3	10^{10}	10^{11}	1.10
Thermoplastic resin	190	25-30		3-4	1017	10^{13}	N/A	
Aluminaberyllia	N/A	5-7 21.0	44.0	8.0	1014			
Aluminum (6061 T-6)	N/A	23.6	200	10	N/A	10^{6}		N/A
Copper (CDA101)	N/A	17.3	400	17	N/A	10^{6}		
Copper-clad Invar	N/A	3-6	150XY/20Z	17-22	N/A	10^{8}		N/A

6.1.1 Categories In general, a PB structure will fit into one of four basic categories of construction: organic base material, nonorganic base material, supporting plane, and constraining core.

6.1.2 Thermal Expansion Mismatch A primary concern when using low expansion surface mount parts is the thermal expansion mismatch between the leadless part and the PB structure. This mismatch will fracture solder joint interconnections if the assembly is subjected to thermal shock, thermal cycling, power cycling and high operating temperatures. The number of fatigue cycles before solder joint failure depends on the thermal expansion mismatch between the part and the PB structure, the temperature range over which the assembly must operate, the solder joint thickness, the size of the part and the power cycling. For example, power cycling may cause an undesirable thermal expansion mismatch if a significant temperature difference exists between a device or package and the PB structure.

6.2 Organic-Base Material Organic-base materials work best with leaded components including leaded chip carriers. With leadless chip carriers and some BGA packaging, the thermal expansion mismatch between package and substrate can cause problems. Also, flatness, rigidity, and thermal conductivity requirements may limit their use. Finally, attention should be paid to package size, I/O count, thermal cycling stability, maximum operating temperature and solder joint compliance.

6.3 Nonorganic Base Materials Nonorganic ceramic base materials typically used with thick-or thin-film technology, although more costly, are suited for leaded and leadless chip carrier designs. Suppliers can incorporate thick-or thin-film resistors directly on the ceramic structure and buried capacitor layers that increase density and improve reliability. However, repairability of the PB structure is limited. Ceramic materials, usually alumina, appear ideal for PB structure with leadless ceramic chip carriers because of their relatively high thermal conductivity. Unfortunately, the structure is limited to approximately 100 mm square. Ceramic PB structures have three primary applications: ceramic hybrid circuits, ceramic multi-chip modules (MCM-L) and ceramic PBs.

6.4 Alternative PB Structures

6.4.1 Supporting-Plane PB Structures Supporting metallic or nonmetallic planes can be used with conventional PBs or with custom processing to enhance PB properties. Depending on the results desired, the supporting plane can be electrically functional or not and can also serve as a structure stiffener, heatsink and/or CTE constraint.

6.4.2 High-Density PB Technology High-density, sequentially processed, multilayer PB structures are available in a wide variety of organic dielectrics. Using thinner copper foils for fabrication the PB manufacturer can provide very narrow conductor and spacing features and by implementing smaller mechanical drills, laser ablation, photo-lithography or plasma processes, smaller blind and/or buried vias can be provided for layer-to-layer interconnections.

The major advantage of this system is that the vias can be as small as 0.10 mm [0.00394 in] or less and conductor widths can range from below 0.12 mm [0.00472 in] for high interconnection density. Thus, some applications can be satisfied with fewer signal layers while providing additional layers for power and ground. Refer to IPC-2226 for more detailed design guidelines for high density PBs.

6.4.3 Constraining Core Structures As with supporting plane, one or more supporting metallic or nonmetallic planes can serve as a stiffener, heatsink, and/or CTE constraint in constraining core structures.

6.4.4 Porcelainized Metal (Metal Core) Structures An integral core of low-expansion metal (for example, copper-clad Invar) can reduce the CTE of porcelainized metal structures so that it closely matches the CTE of the ceramic chip carrier. Also, the structure size is virtually unlimited. However, the low melting point of the porcelain requires low-firing-temperature conductor, dielectric and resistor inks.

7 ASSEMBLY CONSIDERATION FOR MIXED COMPONENT ASSEMBLY

The smaller size of surface mount components, the option of mounting them on one or both sides of the packaging and interconnecting structure, and including through-hole requirements significantly reduces PB real estate. The type of assembly is basically determined by the type of surface mount components to be used. The following shows the relationship and description of types and classes of through-hole, surface mount and intermixed assembly. The class concepts are further defined by prefixing the class with the number 1 or 2 in order to signify components on one or two sides of the PB.

Legend:

Class A = Through-hole component mounting only
Class B = Surface mounted components only
Class C = Simplistic through-hole and surface mounting intermixed assembly
Class X = Complex intermixed assembly, through-hole, surface mount, fine pitch
Class Y = Complex intermixed assembly, through-hole, surface mount, ultra fine pitch, chip scale
Class Z = Complex intermixed assembly, through-hole, ultra fine pitch, COB, flip chip, TAB

7.1 SMT Assembly Process Sequence The SMT assemblies are soldered by reflow (infrared, hot air convection, laser, conduction, vapor phase, and/or wave soldering processes) depending upon the mix of surface mount and through-hole mount components. The process sequence for one-sided SMT is shown in Figure 7-1. Solder paste is applied, components are placed, the assembly is reflow soldered and cleaned. For two-sided SMT assemblies, the PB is turned over and the process sequence just described is repeated. The assembly process for two-sided SMT is simply a sequential combination of SMT processes, however, component weight vs. surface tension should be calculated to determine if heavy components will require additional reinforcement prior to the second reflow soldering process.

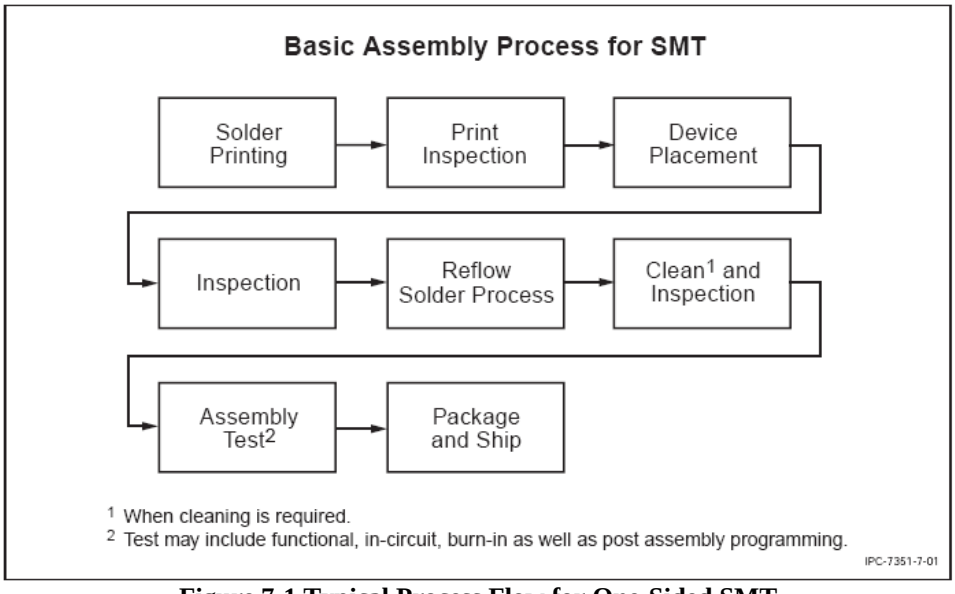


Figure 7-1 Typical Process Flow for One-Sided SMT

The process sequence for surface mount with through-hole or pin-in-hole (PIH) component technology is shown in Figure 7-2. Adhesive is applied and the surface mounted components placed. The adhesive is then cured, and the PB is inverted to receive the through-hole component leads automatically or by hand insertion. After lead clinching (if required), and with the through-hole components on top and the surface mount components beneath, the PB is typically wave soldered. An alternative sequence is to reverse the initial stages i.e., insert (and clinch) the through-hole components before attaching the surface mounted components and then wave soldering.

Finally the assembly may be cleaned, inspected, repaired if necessary, and tested, though not necessarily in that order.

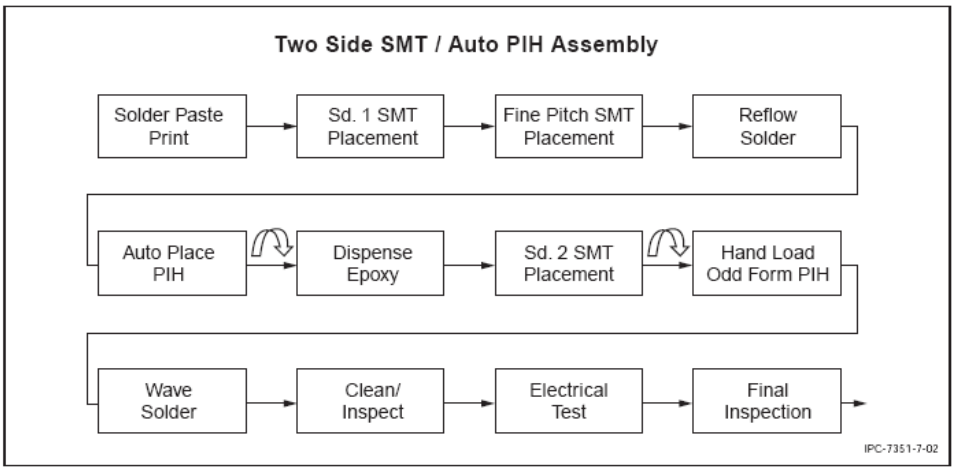


Figure 7-2 Assembly Process Flow for Two-Sided Surface Mount with PIH

7.2 Substrate Preparation

7.2.1 Adhesive Application In wave soldering surface mount components, selection and application of adhesive plays a critical role. With too much adhesive, the adhesive flows onto lands resulting in poor solder fillets. Too little adhesive will fail to accomplish its objective of holding parts to the bottom of the PB during wave soldering.

7.2.2 Conductive Adhesive Some applications for SMT attachment use conductive adhesive as the attachment material. Unlike solder paste which is redistributed when reflowed, conductive adhesives must be properly controlled to ensure joint strength. Also, component placement must be controlled in order to prevent excessive adhesive squeeze-out, and possible shorts to adjacent lands.

7.2.3 Solder Paste Application Solder paste plays an important role in reflow soldering. The paste tacks the component before reflow. It contains flux, solvent, suspending agent, and alloy of the desired composition. Solder paste is applied on the lands before component placement either by screening, stenciling, or syringe. Screens are made from stainless steel or polyester wire mesh, and stencils are etched stainless steel, brass, and other stable alloys. Stencils are preferred for high-volume applications. They are more durable than screens, easier to align, and can be used to apply a thicker layer of solder paste, and, where narrow, point apertures are required for example, for fine-pitch lands. Electroformed stencils may be required for very small components such as 0201 capacitors and resistors.

The goal of the technology that's employed to make the stencil is to ensure that this transfer is as efficient and complete as possible. There are several post processes that enhance the stencil's performance, including electropolishing and trapezoidal section apertures that are created with laser cut technology

7.2.3.1 Laser Cut Stencil Development Laser cut stencils are produced directly from the customer's original Gerber file, IPC-2511 GenCAM or IPC-2581 data. Eliminating the need to make a photo tool eliminates the potential for misregistration. And since there are no photographic steps, a stencil can be made with excellent positional accuracy and remake reproducibility. The tolerance on the aperture dimensions can be held to 7 µm [276 µin], allowing for printing 0.3 mm [0.0118 in] pitch. This process yields maximum paste release, resulting in minimal stencil cleaning, thereby increasing printing efficiency. Plus, the laser cutting process inherently creates trapezoidal apertures, furthering complete paste transfer.

A trapezoidal section aperture is one which has a larger opening on the contact (PB) side of the stencil than on the squeegee side. The opening on the contact side is typically 5 µm [197 µin] per side larger than the squeegee side dimension, depending on the customer's requirements. This wall geometry, when further enhanced by electropolishing, allows for better paste release during the printing process. The results are more noticeable on fine pitch components.

Depending on the overall array design and given the right metal thickness selection, chem-etched stencils can perform adequately at 0.5mm [0.0197 in] pitch. Their efficiency can be improved with performance enhancing processes such as

electropolishing and/or trapezoidal section apertures. For more details in the engineering of the stencil for specific soldering requirements, refer to IPC-7525.

7.2.4 Solder Preforms Solder preforms are sometimes used for through-hole mounted devices as well as SMT rework or prototype PBs. They come in specific size and composition, with flux either inside the preforms, or as a coating or without flux. They may be cost-effective to avoid wave solder processes if there are only a few leaded components on the PB.

7.3 Component Placement The accuracy requirements for device insertion or placement make it more practical to use robotically controlled machines for electronic components on the PB. Selection of the appropriate auto placement machine is dictated by the type of components to be placed or inserted and the assembly production rate. Sequential placement equipment typically utilizes a software controlled X-Y moving table system. Components are individually placed on the PB in succession. Typical cycle times vary with component size and complexity.

7.3.1 Component Data Transfer Prior to designing the PB in the CAD system, each component is constructed in digital form creating an electronic database. The CAD data is most often used to prepare photo-tool artwork, PB fabrication details and assembly instructions but, if developed in the correct format, it can also be adapted to manufacturing processes. Direct transfer of CAD data into automated assembly systems will accelerate production set-up and reduce overall assembly system programming time.

When the CAD database for the device is prepared, specific physical data for each device can be used to assist assembly machine programming for both component placement (X-Y coordinate position) and orientation. To facilitate the X-Y coordinate information, a datum position must be established on the PB surface. The recommended datum ‘‘0’’ for X and Y coordinates ideally, may be one of the global fiducial targets at the lower left or lower right corner of the PB or panel. Surface mount devices are furnished in tape and reel as well as tube magazine feeders to accommodate high-speed assembly systems (tray carriers are most often adapted for fine-pitch components).

Each component is aligned using the body center and a starting orientation for reference. ‘‘0’’ degree is the basic orientation of the device.

Rotational data must be specified from the ‘‘0’’ position in a counter-clockwise direction (typically 90°-180° -270°). The ‘‘0’’ starting position of the component is significant. Tape and reel and JEDEC tray packaged devices for example, have an established standard for orientation.

The tape-and-reel packaged devices have a predetermined orientation that is related to the perforated pattern on one edge of the embossed tape carrier. The standard orientation does vary, however, between unique device families.

Passive and active devices are supplied in a tape and reel format, held and protected within an embossed pocket. Each device family or package type has a standard orientation in relation to the perforated indexing pattern at the tape edge.

Orientation as well as polarity of a device must be defined in the CAD database if the output transferred to assembly systems is to be reliable. Resistors and capacitor devices are common in orientation and have no defined polarity. As the designer develops the component database, numbers are typically assigned to each end of the device to accommodate circuit routing and maintain orientation of value marking or polarity. Tantalum capacitors, diodes, ICs and other polarized components, for example, have unique orientation in relation to tape feed systems. Consider the relationship of the device orientation within the tape cavity to perforation at the tape carrier material edge.

7.4 Soldering Processes Like the selection of automated placement machines, the soldering process selection depends upon the type of components to be soldered and whether or not they will be used in combination with leaded parts. For example, if all components are surface mount types, reflow method (vapor phase, hot air convection or infrared) may be desirable. However, for through-hole and surface mount combinations, in mixed technology, a combination of wave soldering and reflow soldering may be used. No process is best for all soldering tasks. In addition, the number of soldering processes discussed in the following text are by no means complete.

7.4.1 Wave Soldering Wave soldering is an economical method of soldering mass terminations. There are five to six main process variables that must be controlled in the wave soldering process: fluxing, preheat, conveyor speed, conveyor incline, solder temperature, and possibly cooling rate.

In preheat, allowance in the conveyer system must be made for the thermal expansion of the PB during preheating and soldering to prevent PB warpage.

In fluxing, flux density, activity and flux foam/flux spray/ flux wave height must be closely monitored. A system must be in place to determine when the flux activity has deteriorated and when the old flux must be replaced and the new flux added. Speed is the time sequence and duration of all of the steps in soldering. By controlling the speed, more uniform and better joints result. In controlling the conveyer speed, preheating a packaging and interconnecting assembly in two or three stages

minimizes the thermal shock damage to the assembly and improves its service life. Uniform preheating is achieved by developing a solder schedule that specifies preheat settings and conveyer speed for each type of PB.

The solder wave is an important variable. Wave geometry is especially important for preventing icicles and bridges and for the proper soldering of surface mounted components. Wave geometries include uni-directional and bi-directional; single and double; rough, smooth and dead zone; oil intermix, dry, and bubbled, and with or without a hot air knife. Special solder waves just for surface mounted components are also available.

The concern generally expressed in wave soldering of surface mount devices is damage to the components when they go through the soldering wave at 260 °C [500 °F]. The maximum shift in tolerance of resistors and capacitors is generally found to be 0.2%. This is a negligible amount considering the part tolerance of commonly used components is 5% to 20%. The components generally spend about three seconds in the wave but they are designed to withstand soldering temperatures of 260 °C [500 °F] for up to ten seconds.

In wave soldering, outgassing and solder skips are two other main concerns. The outgassing or gas evolution occurs on the trailing terminations of chip resistors and capacitors. It is believed to be caused by insufficient drying of flux and can be corrected by raising the packaging and interconnecting assembly preheat temperature or time. The other concern, solder skips, is caused by the shadow effect of the part body on the trailing terminations. Orienting the part in such a way that both terminations are soldered simultaneously solves most shadow effect problems. Some manufacturers use an extra land to serve as a ‘‘solder thief’’ for active components.

The most common method for solving both outgassing and shadow effect is by switching to the dual wave system where the first wave is turbulent and the second wave is laminar. The turbulent wave serves to provide an adequate amount of solder across the surface of the packaging and interconnecting structure in order to help eliminate outgassing and solder skips. The laminar wave is used to help eliminate icicles and bridging.

7.4.2 Vapor Phase (VP) Soldering Vapor phase soldering, also known as condensation soldering, uses the latent heat of vaporization of an inert liquid for soldering. The latent heat is released as the vapor condenses on the part to be soldered. The soldering temperature is constant and is controlled by the type of fluid.

Unlike wave, IR, convection and laser soldering, vapor phase soldering does not require control of the heat input to the solder joints or to the PB. It heats independently of the part geometry, heats uniformly, and does not exceed the fluid boiling temperature. This process is also suitable for soldering odd-shaped parts, flexible circuits, and pins and connectors, as well as for reflow of tin-lead electroplate and surface mount packages. Since heating is by condensation, the rate of temperature rise depends on the mass of the part. Therefore, the leads on the package in contact with the packaging and interconnecting structure heat up faster than the component body. This may lead to wicking of the solder up the lead. Before exposing the loaded assembly to VP reflow process, preheating the assembly is highly recommended to avoid thermal shock to components and the PB.

7.4.3 IR Reflow Soldering In infrared (IR) reflow soldering, the radiant or convective energy is used to heat the assembly. There are basically two types of IR reflow methods, either focused (radiant) or non-focused (convective). The latter is proving more desirable for SMT. The focused IR radiates heat directly on the parts and may unevenly heat assemblies. The heat input on the part may also be color-dependent. In non-focused or diffused IR, the heating medium can be air or an inert gas or simply the convection energy. A gradual heating of the assembly is necessary to drive off volatiles from the solder paste. After an appropriate time in preheat, the assembly is raised to the reflow temperature for soldering and then cooled.

7.4.4 Hot Air/Gas Convection Soldering The reflow process affects soldering by transporting the PBs through a stream of heated gas (e.g., air, nitrogen). Heat is transferred to the components and PB by conduction from the gas. Because the PBs do not receive significant direct radiation from the heating source, convection soldering avoids the shadowing problems that can occur with infrared soldering machines, especially short wavelength (lamp) versions. This enables more uniform heating and a higher component density on the PB compared to other mass reflow soldering methods. The gas temperature controls the maximum temperature that can be seen by the assembly.

Use of a nitrogen atmosphere permits better thermal coupling between the circulating gas and the component terminations. In addition to improved wetting, the process window for double-sided reflow is enlarged, and lower activated solder paste flux can be used.

7.4.5 Laser Reflow Soldering Laser soldering complements other mass soldering processes rather than replacing them and, as with in-line reflow soldering, lends itself well to automation. It is faster than hand soldering but not as fast as wave, vapor, IR soldering or hot air convection. Heat-sensitive components that may be damaged in reflow processes can be soldered by laser. Process problems include thermal damage to surrounding areas and solder balls.

7.4.6 Conduction Reflow Soldering Conduction reflow affects soldering through the transference of heat from beneath the PB. This can have advantages with high mass components, temperature sensitive components and metal backed assemblies. In

comparison with other solder processes, the slightly slower heating and cooling ramp times caused by heat spreading through the PB substrates can provide a reduction of thermal shock and improved resistance against rapid cooling issues such as tombstoning. Though in-line conduction reflow ovens are available, the most common use of conductive reflow is in ‘‘hot plate’’ rework systems.

For more detail regarding reflow soldering refer to IPC-7530.

7.5 Cleaning Flux requiring solvent cleaning—synthetic or rosin-based fluxes are generally known as synthetic activated (SA), synthetic mildly activated (SMA), rosin activated (RA) or rosin mildly activated (RMA). Stabilized halogenated hydrocarbon/alcohol azeotropes are the preferred solvents for removal of synthetic and rosin-based flux residues.

7.6 Repair/Rework The repair/rework of PB assemblies requires special care in design and practice. Because of the small land geometries, heat applied to the PB should be minimized. There are various tools available for removing components. Resistance heating tweezers are usually used for removing surface mounted components. Various types of hot air/gas and IR systems are also used for removing surface mounted components. One of the main issues when using hot air/gas devices is preventing damage to adjacent components. Refer to IPC7711/21. There are four basic requirements for a successful rework; good PB design layout, selection of the correct rework equipment or tools, sufficient manual skill, and adequate training.

Successful removal of large multi-leaded integrated circuit packages involves the use of hot gas or heated electrode tools. Sufficient clearance around the package to permit the re-work is essential. Clearance should be provided completely around the device as identified in the standards as the ‘‘courtyard manufacturing zone.’’

7.6.1 Heatsink Effects Large ground planes or heatsinks will conduct heat away from the component being reworked if present in a PB substrate. Extra heat, perhaps for longer periods, is then required which, in turn, can lead to damage to components or the PB. The fact that the solder joints may not reach reflow temperature is no guarantee that the component or the PB have not been overheated. Heatsinking effects are a design problem which must be tackled at the PB layout stage. Whenever possible, any component termination which may not rework, including leaded-through hole type, should be thermally isolated from any ground plane or integral heat-sink by a short length of copper conductor.

7.6.2 Dependence on PB Material Type To ensure minimum damage to the PB during rework, base laminate should be a good quality resin and reinforcement type from a high copper peel strength material. High packing density is required. The use of inferior laminates can easily lead to problems with lands peeling away during rework. This may result in either scrapping of complete assemblies or expensive repair of damaged copper area. For PBs having high thermal mass such as middle-core types or those with large area ground planes, to avoid employing a tool with high heat input rate, the use of a hot plate to provide background heating is essential.

7.6.3 Dependence on Copper Land and Conductor Layout The space on a PB is at a premium or single conductors must be kept very short. Designers will often route a conductor between adjacent device land space at a pitch of the component device being placed. In such cases, conductors should be covered with a solder mask to minimize the risk of lifting conductors during rework operations. Figure 7-3

Figure 7-3 Feature Pitch and Conductor Per Channel Combinations

8 IPC-7252 DISCRETE COMPONENTS

Lead terminations **shall** be coated with a finish that provides protection and maintains solderability. Evaluations of lead terminations **shall** use the methods described in IPC-J-STD-002. Test A/A1 and Test D **shall** be used as a default, unless otherwise agreed upon between user and supplier. The user and supplier will need to agree on the coating durability requirements as defined in IPC-J-STD-002. If this is not provided, Typical Coating Durability Category 3 from IPC-J-STD-002 becomes the default condition for the surface finishes as shown in Table 8-1.

Table 8-1 Solderability Tests for Axial Leaded Components

Test A/A1 of J-STD-002	Test D of J-STD-002	Steam Aging Default
Solder Bath/Dip and Look Test (Leaded Components and Stranded Wire)	Resistance to Dissolution/ Dewetting of Metallization Test	Category 3 - 8 hours ± 15 min. Steam Conditioning

Plating may consist of a tin/lead alloy or a lead free equivalent. If tin/lead is used the solder should contain between 58 to 68% tin. Any coating may be applied to the lead finish by hot dipping or by plating from solution. Plated leads should be subjected to a post plating reflow operation to fuse the solder. If tin/lead finish is used it should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

Discrete component packages are normally processed using standard wave solder processes. In addition, parts should be capable of withstanding ten cycles through a standard reflow system, particularly if surface mount parts are added after the through-hole parts have been attached. Each cycle shall consist of 10 to 30 seconds or 20 to 40 seconds within 5 ºC of peak temperature for tin/lead or lead free, respectively.

If a reflow process is used the requirements of IPC/JEDEC J-STD-020 shows the appropriate reflow cycles and profiles for the reflow conditions as shown in Table 8-2. In addition the Moisture Sensitivity Level (MSL) **shall** be defined per J-STD-020, so that the floor life of the component is properly established.

Table 8-2 Package Peak Reflow Temperatures

Reflow Conditions	**Pkg. Thickness ≥ 2.5 mm or Pkg. Volume ≥ 350 mm^3**	**Pkg. Thickness <2.5 mm and Pkg. Volume <350 mm^3**
Tin/Lead Eutectic	Convection 225 +0/-5°C	Convection 240 +0/-5°C
Lead Free	Convection 245 +0 °C	Convection 260 +0 °C

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and or non-integral heat sinks.
Note 2: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 3: Components intended for use in a ‘‘lead-free’’ assembly process shall be evaluated using the ‘‘lead free’’ peak temperature and profiles defined

8.1 Axial Leaded Components The axial lead component family includes resistors, capacitors, diodes and inductors. Axial leaded components are through-hole components that have the lead wire extending from the component body, or module body, along its longitudinal axis. The leads normally come out in a straight line and must be bent. They enter the holes in the PB perpendicular to the body of the component. The component is horizontally mounted with the component body parallel to the printed bard surface. When bending the leads care must be taken to avoid damaging the seal where the lead connects to the component body. When mounting axial leaded parts, the designer should space the holes at a sufficient distance to avoid bending the lead too close to the body of the component. The goal being that the body of the component should be approximately centered between the two mounting holes.

8.1.1 Axial Leaded Resistors (Round Body)

Figure 8-1 Axial Resistor

8.1.2 Axial Leaded Resistors (Square Body)

8.1.3 Axial Leaded Capacitors (Non-Polarized, Polarized)

Figure 8-X Axial Capacitor

8.1.4 Axial Leaded Diodes (Square, Oval, Round)

Figure 8-X Axial Diode

8.1.5 Axial Leaded Inductors (Square, Oval, Round)

8.2 Radial Leaded Components

The radial leaded component family includes resistors, capacitors, diodes, crystals, test points, and inductors

Radial leaded components may have two or more leads exiting from the body. The leads usually come from the same surface and bending may not be necessary as the leads can be inserted directly into the holes of the PB. The lead spacing of radial leaded components varies greatly, so the hole spacing is usually predicated by the exit of the leads from the body of the component. When the lead spacing is too close for the clearance requirements, the leads may normally be spread in order to provide a good connection into the plated-through holes, or a stress relief bend added to the lead forming.

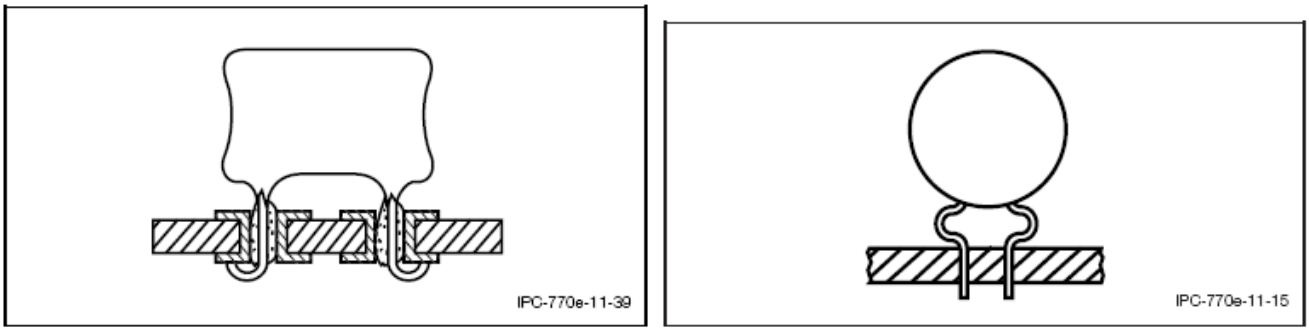


Figure 8 Radial Leaded Components

8.2.1 Radial Leaded Capacitors (Square, Oval, Round)

Figure 8-X

Figure 8-X

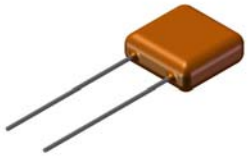


Figure 8-X

9 IPC-7253 DUAL INLINE-PACKAGE (DIP)

The DIP is an excellent example of a multiple leaded radial part. The leads of the DIP need not be bent to enter the component holes because the part was specially designed to avoid having to perform the pre-bend operation. The dual in-line package was developed using [0.100 in] pitch with the spacing between the two rows usually considered at [0.300 in]. The parts are provided using a plastic body encapsulating a lead frame to which the die is attached. The moisture sensitivity concepts of plastic parts need to be taken into consideration.

In some applications the DIP body has been configured where the die has been hermetically sealed. The package body was thus made of ceramic material. The CERDIP has the same physical characteristics as its plastic counterpart.

DIP packages are normally processed using standard wave solder processes. In addition, parts should be capable of withstanding ten cycles through a standard reflow system, particularly if surface mount parts are added after the through-hole parts have been attached. Each cycle shall consist of 10 to 30 seconds or 20 to 40 seconds within 5 ºC of peak temperature for tin/lead or lead free, respectively.

End terminations **shall** be coated with a finish that provides protection and maintains solderability. Evaluations of terminations **shall** use the methods described in IPC-J-STD-002. Test B/B1 and Test D **shall** be used as a default, unless otherwise agreed upon between user and supplier. The user and supplier will need to agree on the coating durability requirements as defined in IPC-J-STD-002. If this is not provided, Typical Coating Durability Category 3 from IPC-J-STD-002 becomes the default condition for the surface finishes as shown in Table 9-1.

Table 9-1 Solderability Tests for DIP Components

Test B/B1 of J-STD-002	Test D of J-STD-002	Steam Aging Default
Solder Bath/Dip and Look Test (Leadless Components)	Resistance to Dissolution/ Dewetting of Metallization Test	Category 3 - 8 hours ± 15 min. Steam Conditioning

Plating may consist of a tin/lead alloy or a lead free equivalent. If tin/lead is used the solder should contain between 58 to 68% tin. Any coating may be applied to the termination by hot dipping or by plating from solution. Plated terminations should be subjected to a post plating reflow operation to fuse the solder. If tin/lead finish is used it should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.
The following sections for each component family provide information on basic component construction, termination materials, marking, carrier package format and resistance to soldering.

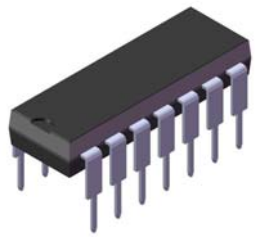


Figure 9-1 Packaging of DIP Components

Parts should be capable of withstanding five cycles through a standard reflow system. Each cycle shall consist of 10 to 30 seconds or 20 to 40 seconds within 5 ºC of peak temperature for tin/lead or lead free, respectively.

Parts must also be capable of withstanding a minimum duration immersion in molten solder at the time and temperature shown in Table 9-2. If a reflow process is used the requirements of IPC/JEDEC J-STD-020 shows the appropriate reflow cycles and profiles for the reflow conditions as shown in Table 9-3.

Table 9-2 Solderability, Bath Method: Test Severities (duration and temperature)

Alloy Composition	Severity					
	(215 +/- 3) °C (3+/ 0.3)s	(10+/- 1)s	(235 +/- 5) °C (2+/ 0.2)s	(5+/- 0.5)s	(245 +/- 5) °C (3+/ 0.3)s	(250 +/- 5) °C (3+/ 0.3)s
SnPb	X	X	X	X		
Sn96.5Ag3.0Cu0.5					X	
Sn99.3Cu0.7						X

Alloy composition for test purposes only. The solder alloys consist of 3.0 wt% to 4.0 wt% Ag, 0.5 wt% to 1.0 wt% Cu, and the remainder of Sn may be used instead of Sn96.5Ag3.0Cu0.5. The solder alloys consist of 0.45 wt% to 0.9 et% Cu and the remainder of Sn may be used instead of Sn99.3Cu0.7

NOTE 1: "X" denotes "applicable'
NOTE 2: Refer to IPC-J-STD-006 to identify alloy composition
NOTE 3: The basic lead free solder alloys listed in this table represent compositions that are currently preferred for lead free soldering processes. If solder alloys other than those listed here are used, it should be verified that the given severities are applicable.

Table 9-3 Package Peak Reflow Temperatures

Reflow Conditions	Pkg. Thickness ≥ 2.5 mm or Pkg. Volume ≥ 350 mm^3	Pkg. Thickness <2.5 mm and Pkg. Volume <350 mm^3
Tin/Lead Eutectic	Convection 225 +0/-5°C	Convection 240 +0/-5°C
Lead Free	Convection 245 +0 °C	Convection 260 +0 °C

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and or nonintegral heat sinks.
Note 2: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 3: Components intended for use in a ''lead-free'' assembly process shall be evaluated using the ''lead free'' peak temperature and profiles defined

9.1 Dual In-Line I/C

9.2 Dual In-Line Resistor Networks

9.3 Dual In-Line Sockets

10 IPC-7254 THREE LEADED SEMICONDUCTORS

Lead terminations **shall** be coated with a finish that provides protection and maintains solderability. Evaluations of lead terminations **shall** use the methods described in IPC-J-STD-002. Test A/A1 and Test D **shall** be used as a default, unless otherwise agreed upon between user and supplier. The user and supplier will need to agree on the coating durability requirements as defined in IPC-J-STD-002. If this is not provided, Typical Coating Durability Category 3 from IPC-J-STD-002 becomes the default condition for the surface finishes as shown in Table 10-1.

Table 10-1 Solderability Tests for Header Components

Test A/A1 of J-STD-002	Test D of J-STD-002	Steam Aging Default

Solder Bath/Dip and Look Test (Leaded Components and Stranded Wire)	Resistance to Dissolution/ Dewetting of Metallization Test	Category 3 - 8 hours ± 15 min. Steam Conditioning

Plating may consist of a tin/lead alloy or a lead free equivalent. If tin/lead is used the solder should contain between 58 to 68% tin. Any coating may be applied to the lead finish by hot dipping or by plating from solution. Plated leads should be subjected to a post plating reflow operation to fuse the solder. If tin/lead finish is used it should be at least 0.0075 mm [0.0003 in] thick.

The plated leads **shall** be symmetrical, and **shall** not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination **shall** cover the ends of the components, and **shall** extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes **shall** have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

Parts should be capable of withstanding five cycles through a standard reflow system. Each cycle shall consist of 10 to 30 seconds or 20 to 40 seconds within 5 ºC of peak temperature for tin/lead or lead free, respectively.

Parts must also be capable of withstanding a minimum duration immersion in molten solder at the time and temperature shown in Table 10-2. If a reflow process is used the requirements of IPC/JEDEC J-STD-020 shows the appropriate reflow cycles and profiles for the reflow conditions as shown in Table 10-3. In addition the Moisture Sensitivity Level (MSL) **shall** be defined per J-STD-020, so that the floor life of the component is properly established.

Table 10-2 Solderability, Bath Method: Test Severities (duration and temperature)

Alloy Composition	**Severity**					
	(215 +/- 3) °C (3+/ 0.3)s	**(10+/- 1)s**	**(235 +/- 5) °C (2+/ 0.2)s**	**(5+/- 0.5)s**	**(245 +/- 5) °C (3+/ 0.3)s**	**(250 +/- 5) °C (3+/ 0.3)s**
SnPb	**X**	**X**	**X**	**X**		
Sn96.5Ag3.0Cu0.5					**X**	
Sn99.3Cu0.7						**X**

Alloy composition for test purposes only. The solder alloys consist of 3.0 wt% to 4.0 wt% Ag, 0.5 wt% to 1.0 wt% Cu, and the remainder of Sn may be used instead of Sn96.5Ag3.0Cu0.5. The solder alloys consist of 0.45 wt% to 0.9 et% Cu and the remainder of Sn may be used instead of Sn99.3Cu0.7

NOTE 1: "X" denotes "applicable"
NOTE 2: Refer to IPC-J-STD-006 to identify alloy composition
NOTE 3: The basic lead free solder alloys listed in this table represent compositions that are currently preferred for lead free soldering processes. If solder alloys other than those listed here are used, it should be verified that the given severities are applicable.

Table 10-3 Package Peak Reflow Temperatures

Reflow Conditions	**Pkg. Thickness ≥ 2.5 mm or Pkg. Volume ≥ 350 mm^3**	**Pkg. Thickness <2.5 mm and Pkg. Volume <350 mm^3**
Tin/Lead Eutectic	Convection 225 +0/-5°C	Convection 240 +0/-5°C
Lead Free	Convection 245 +0 °C	Convection 260 +0 °C

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and or non-integral heat sinks.
Note 2: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 3: Components intended for use in a ''lead-free'' assembly process shall be evaluated using the ''lead free'' peak temperature and profiles defined

10.1 TO 220

10.2 TO 92

10.3 TO5

10.4 TO3 Power Transistor

It is recommended that copper lands fully circumscribe both the plated-through holes as well as the unsupported holes used to fasten the transistor to the PB. In some configurations the land in the mounting site must be connected to ground as a part of the component condition (see Figure 10-x).

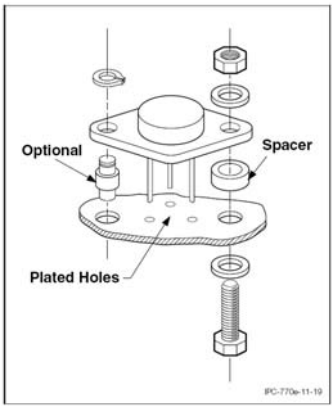


Figure 10-X Mechanically Secured Power Transistor

11 IPC-7255 MULTIPLE LEADED SEMICONDUCTORS

This device family includes multiple lead variable resistors and pin grid arrays.

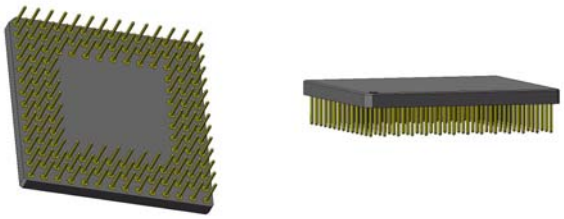


Figure 11-1 Pin Grid Array

Lead terminations **shall** be coated with a finish that provides protection and maintains solderability. Evaluations of lead terminations **shall** use the methods described in IPC-J-STD-002. Test A/A1 and Test D **shall** be used as a default, unless otherwise agreed upon between user and supplier. The user and supplier will need to agree on the coating durability requirements as defined in IPC-J-STD-002. If this is not provided, Typical Coating Durability Category 3 from IPC-J-STD-002 becomes the default condition for the surface finishes as shown in Table 11-1.

Table 11-1 Solderability Tests for Pin Grid Arrays

Test A/A1 of J-STD-002	Test D of J-STD-002	Steam Aging Default
Solder Bath/Dip and Look Test (Leaded Components and Stranded Wire)	Resistance to Dissolution/ Dewetting of Metallization Test	Category 3 - 8 hours ± 15 min. Steam Conditioning

Plating may consist of a tin/lead alloy or a lead free equivalent. If tin/lead is used the solder should contain between 58 to 68% tin. Any coating may be applied to the lead finish by hot dipping or by plating from solution. Plated leads should be subjected to a post plating reflow operation to fuse the solder. If tin/lead finish is used it should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

Parts should be capable of withstanding ten cycles through a standard reflow system. Each cycle shall consist of 10 to 30 seconds or 20 to 40 seconds within 5 ºC of peak temperature for tin/lead or lead free, respectively.

Parts must also be capable of withstanding a minimum duration immersion in molten solder at the time and temperature shown in Table 11-2. If a reflow process is used the requirements of IPC/JEDEC J-STD-020 shows the appropriate reflow cycles and profiles for the reflow conditions as shown in Table 11-3. In addition the Moisture Sensitivity Level (MSL) **shall** be defined per J-STD-020, so that the floor life of the component is properly established.

Table 11-2 Solderability, Bath Method: Test Severities (duration and temperature)

Alloy Composition	Severity

	(215 +/- 3) °C (3+/ 0.3)s	(10+/- 1)s	(235 +/- 5) °C (2+/ 0.2)s	(5+/- 0.5)s	(245 +/- 5) °C (3+/ 0.3)s	(250 +/- 5) °C (3+/ 0.3)s
SnPb	**X**	**X**	**X**	**X**		
Sn96.5Ag3.0Cu0.5					**X**	
Sn99.3Cu0.7						**X**

Alloy composition for test purposes only. The solder alloys consist of 3.0 wt% to 4.0 wt% Ag, 0.5 wt% to 1.0 wt% Cu, and the remainder of Sn may be used instead of Sn96.5Ag3.0Cu0.5. The solder alloys consist of 0.45 wt% to 0.9 et% Cu and the remainder of Sn may be used instead of Sn99.3Cu0.7

NOTE 1: "X" denotes "applicable"
NOTE 2: Refer to IPC-J-STD-006 to identify alloy composition
NOTE 3: The basic lead free solder alloys listed in this table represent compositions that are currently preferred for lead free soldering processes. If solder alloys other than those listed here are used, it should be verified that the given severities are applicable.

Table 11-3 Package Peak Reflow Temperatures

Reflow Conditions	**Pkg. Thickness ≥ 2.5 mm or Pkg. Volume ≥ 350 mm^3**	**Pkg. Thickness <2.5 mm and Pkg. Volume <350 mm^3**
Tin/Lead Eutectic	Convection 225 +0/-5°C	Convection 240 +0/-5°C
Lead Free	Convection 245 +0 °C	Convection 260 +0 °C

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and or non-integral heat sinks.
Note 2: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 3: Components intended for use in a ''lead-free'' assembly process shall be evaluated using the ''lead free'' peak temperature and profiles defined

11.1 Pin Grid Array

12 IPC-7256 UNIQUE MULTIPLE FUNCTION PARTS

12.1 Termination Materials End terminations **shall** be coated with a finish that provides protection and maintains solderability. Evaluations of end terminations **shall** use the methods described in IPC-J-STD-002. Test A/A1 and Test D **shall** be used as a default, unless otherwise agreed upon between user and supplier. The user and supplier will need to agree on the coating durability requirements as defined in IPC-J-STD-002. If this is not provided, Typical Coating Durability Category 3 from IPC-J-STD-002 becomes the default condition for the surface finishes as shown in Table 12-1.

Table 12-1 Solderability Tests for Mounting Holes

Test A/A1 of J-STD-002	**Test D of J-STD-002**	**Steam Aging Default**
Solder Bath/Dip and Look Test (Leaded Components and Stranded Wire)	Resistance to Dissolution/ Dewetting of Metallization Test	Category 3 - 8 hours ± 15 min. Steam Conditioning

Plating may consist of a tin/lead alloy or a lead free equivalent. If tin/lead is used the solder should contain between 58 to 68% tin. Any coating may be applied to the lead finish by hot dipping or by plating from solution. Plated leads should be subjected to a post plating reflow operation to fuse the solder. If tin/lead finish is used it should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

The parts should be capable of withstanding ten cycles through a standard reflow system. Each cycle shall consist of 10 to 30 seconds or 20 to 40 seconds within 5 ºC of peak temperature for tin/lead or lead free, respectively.

Parts must also be capable of withstanding a minimum duration immersion in molten solder at the time and temperature shown in Table 12-2. If a reflow process is used the requirements of IPC/JEDEC J-STD-020 shows the appropriate reflow cycles and profiles for the reflow conditions as shown in Table 12-3. In addition the Moisture Sensitivity Level (MSL) **shall** be defined per J-STD-020, so that the floor life of the component is properly established.

Table 12-2 Solderability, Bath Method: Test Severities (duration and temperature)

Alloy Composition	**Severity**

	(215 +/- 3) °C (3+/ 0.3)s	(10+/- 1)s	(235 +/- 5) °C (2+/ 0.2)s	(5+/- 0.5)s	(245 +/- 5) °C (3+/ 0.3)s	(250 +/- 5) °C (3+/ 0.3)s
SnPb	**X**	**X**	**X**	**X**		
Sn96.5Ag3.0Cu0.5					**X**	
Sn99.3Cu0.7						**X**

Alloy composition for test purposes only. The solder alloys consist of 3.0 wt% to 4.0 wt% Ag, 0.5 wt% to 1.0 wt% Cu, and the remainder of Sn may be used instead of Sn96.5Ag3.0Cu0.5. The solder alloys consist of 0.45 wt% to 0.9 et% Cu and the remainder of Sn may be used instead of Sn99.3Cu0.7

NOTE 1: "X" denotes "applicable"
NOTE 2: Refer to IPC-J-STD-006 to identify alloy composition
NOTE 3: The basic lead free solder alloys listed in this table represent compositions that are currently preferred for lead free soldering processes. If solder alloys other than those listed here are used, it should be verified that the given severities are applicable.

Table 12-3 Package Peak Reflow Temperatures

Reflow Conditions	**Pkg. Thickness ≥ 2.5 mm or Pkg. Volume ≥ 350 mm^3**	**Pkg. Thickness <2.5 mm and Pkg. Volume <350 mm^3**
Tin/Lead Eutectic	Convection 225 +0/-5°C	Convection 240 +0/-5°C
Lead Free	Convection 245 +0 °C	Convection 260 +0 °C

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and or non-integral heat sinks.
Note 2: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 3: Components intended for use in a ''lead-free'' assembly process shall be evaluated using the ''lead free'' peak temperature and profiles defined

12.1 Crystal

12.2 Oscillator

13 IPC-7257 CONNECTORS AND HEADERS (Clearance, Press Fit)

13.1 Header, Single Row

13.2 Header, Multiple Row

Figure 13-2 Multiple Row Header

14 IPC-7258 SINGLE IN-LINE PACKAGE (SIP) RESISTOR NETWORKS

15 IPC-7259 MOUNTING HARDWARE

16 ZERO COMPONENT ORIENTATIONS

The zero component orientations expressed in IPC-7251 are defined in terms of the standard component CAD library with respect to a given PB design. Recognizing that a single land pattern may be used for the same component part from different suppliers and that each component supplier may have different orientations on their reels or that the components may come in trays, there exists the possibility that the PB designer loses the ability to reference a single land pattern if the zero rotation of a part is according to the method the component is delivered to the assembly machine. Since the CAD library contains a single land pattern, the zero component rotation is thus defined according to the CAD library. Subsequently, component suppliers can identify the orientation of the parts on the reels by associating the placement of the part on the reel to zero orientations defined in IPC-7251. If pin 1 is at the lower left as defined by the pick and place machine tape and reel, for example, then the component on the reel is rotated 90° counterclockwise from the zero rotation given in IPC-7251. Standardizing the orientation of components for

the installation and utilization of various packaging methods, such as tubes, trays or tapes and reels, among the variations of automated assembly equipment existing today is outside the scope of this document.

Figure 16-1 lists the most commonly used parts and their proper zero component rotation.

1) Axial Lead Capacitors, Resistors, Diodes and Inductors (RES, CAP, DIO and IND) – **Pin 1 (Positive or Cathode) on Left**

2) Radial Lead Capacitors (CAP) – **Pin 1 (Positive) on Left**

3) Dual-in-line Packages (DIP) – **Pin 1 Left - Upper**

4) Pin Grid Array (PGA) – **Pin 1 Left – Upper**

5) Unique Components – **Pin 1 Left – Upper**

6) Headers (HDR) – **Pin 1 Left - Upper**

Figure 16-1 Zero Component Rotations for Common Through-Hole Package Outlines

APPENDIX A
IPC Land Pattern Viewer

The IPC Land Pattern Viewer, hereafter referred to as the IPC LP Viewer, is a shareware program that allows users to view component and land pattern dimensional data in tabular form as well as graphical images that illustrate how a component is attached to the land pattern on the PB. The IPC LP Viewer is provided on a CD-ROM that is included with the IPC-7251 standard. Updated versions of the program, including dimensional data for new component families, can be downloaded for free from www.ipc.org under the ‘‘PCB Tools and Calculators’’ link.

A.1 Software Installation The IPC LP Viewer comes on CD-ROM in a zipped file format (updated versions of the IPC LP Viewer can also be downloaded from www.ipc.org under the ‘‘PCB Tools and Calculators’’ link). The zip file contains important text files on the usage of the shareware program as well as installation requirements. Microsoft .NET Framework is required for the IPC LP Viewer to run properly. If you have determined that you do not have this component, the installation requirement text file details how to obtain this software. Once you have confirmed that your system has Microsoft .NET Framework, you can select the executable IPC LP Viewer file to begin the installation process. See the Users Guide within the IPC LP Viewer for detailed instructions on the download of .NET Framework.

Note: A special file is required for the eventual build of user preferences which provides for the addition, deletion and arrangement of land pattern library documentation files; this file has the extension [.dat]. The IPC LP Viewer program installation does not initially include a [.dat] file and therefore one is created automatically (default.dat) the first time you run the program. When starting the program for the first time, the User will be prompted by a message that states a .DAT file does not exist and that one is being created. A second message will be displayed confirming that the file has been created.

A.2 Software Usage Once installed, select the ‘‘Users Guide’’ tool bar button located on the main interface screen for the IPC LP Viewer. This .pdf document helps in familiarizing the user with the Viewer by providing detailed information on the following:

- Software Installation
- Setting up User Preferences
- Operating the Search Library Menu
- Updating Parts Library Files

A.3 Software Updates The IPC LP Viewer relies on library files for component and land pattern dimensional data. The extension for the library files is [.plb]. These .plb files provide the raw dimensional data necessary for the software to display components and land patterns in graphical forum. For example, there is a separate .plb file for the three land pattern geometries established in this standard, and this includes ThA.plb for Density Level A, ThB.plb for Density Level B, and Thc.plb for Density Level C.

.plb files also contain parts attributes. Attributes hold vital statistical and descriptive data that every land pattern needs so other users can quickly identify the component characteristics. Attributes help organize data used to search for existing library parts. Detailed descriptions of how to utilize attributes can be found by selecting the ‘‘Users Guide’’ tool bar button located on the main interface screen for the IPC LP Viewer.

As new component families are standardized by the industry, new .plb library files will be made available to users of the IPC LP Viewer. These updated .plb files can be downloaded for free from www.ipc.org under the ‘‘PCB Tools and Calculators’’ link.

A.4 Software Upgrades The IPC LP Viewer is a shareware program that allows users to search and display existing land patterns for standardized component families. The Viewer is supported by additional, commercial software tools that allow for the calculation of new land patterns as well as the creation of new part libraries that stores new component and land pattern data. Information on these enhanced software tools is available at www.ipc.org under the ‘‘PCB Tools and Calculators’’ link.